Design of a Domino Logic Using PMOS Footer Circuit

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Abstract—A new PMOS stack in footer circuit technique has been proposed for leakage current reduction and speed enhancement of domino logic circuits. The threshold voltage of the PMOS transistor is increased in footer circuit to increase the resistance in standby mode. This technique reduces the power reduction of the circuit by 57% by previous domino logic circuit design. To use PMOS transistor in footer circuit can make a little variation in the size of the overall circuit.

Keywords—CMOS, PMOS Stack, Domino Logic, Footer circuit.

I. INTRODUCTION
Conventional VLSI Designers have different options to reduce the power of the circuit for their designs. But the current semiconductor industry using millions of transistor on small area which is invoking the new sources of power consumption such as leakage current in standby mode of transistor. There are many approaches to reduce the power dissipation of the circuit at various design stages and different design techniques have been proposed. Leakage currents with sub-threshold source-to-drain leakage, reverse bias junction band-to-band tunneling, gate oxide tunneling, and other current drawn continuously from the power supply cause static power dissipation [1]. To reduce dynamic power dissipation it is necessary to reduce the supply voltage of the circuit, reduction of supply voltage after a certain limit affects the performance of the circuit [2], to maintain circuit performance of the circuit it is necessary to decrease the threshold voltage as well, but it leads to leakage power dissipation. Leakage power can be reduced by increasing the threshold voltage [3]. In this paper the leakage current is reducing in pull down network on the Circuit. For the suggested technique uses Two PMOS in Pull Down network.

Challenges in the design of Standard Domino circuits are reviewed in Section II; this section specially gives an overview of the existing designs. The operation of the proposed domino logic with two PMOS in footer circuit technique is described in Section III. Simulation results characterizing the delay, power and power delay product of the proposed techniques compared to Standard Domino and Previous work are presented in Section IV in this section special focus is on the comparison of the different technology for the specified design. Finally the conclusion is given in Section V.

II. EXISTING DOMINO LOGIC CIRCUITS
A. Standard Domino Logic
A standard footed domino gate is shown in Fig. 1. Domino circuits behave in the following manner. When the clock signal is low, the domino logic circuit is in the precharge phase. During this phase, the dynamic node is charged to VDD1 by the pull-up transistor. The output transitions low, turning on the keeper transistor. The output transitions low, turning on the keeper transistor. When the clock transitions high, the circuit enters the evaluation phase. In this...
phase, provided that the necessary input combination to discharge the dynamic node is applied, the circuit evaluates and the dynamic node is discharged to ground. If the circuit does not evaluate in the evaluation phase, the high state of the dynamic node is preserved against coupling noise, charge sharing, and sub threshold leakage current by the keeper transistor until the pull up transistor is turned on at the beginning of the following precharge phase. The foot transistor (see Fig. 1) controlled by the clock signal divides the operation of a domino logic circuit into two distinct phases independent of the timing of the input signals. The isolation of the pull down network from ground in the precharge phase eases the relative timing of the input and clock signals in cascaded multistage footed domino circuits. If the necessary input combination to discharge the dynamic node is applied during the precharge phase, the pull down transistors cannot alter the state of the dynamic node as the pull down path to ground is blocked by the foot transistor. The foot transistor has a nonzero resistance and parasitic capacitance that degrades the evaluation speed of a domino circuit. The foot transistor is typically sized significantly larger than the pull down network transistors to minimize this speed degradation. Increasing the size of the foot transistor, however, increases the power dissipation since the foot transistor switches every clock cycle.

One of the major advantages of the domino logic over the static CMOS is that this works on high frequency clock and there is no PUN so this eliminates the spurious transitions and corresponding power dissipation. But in some logical conditions output is pre-charged only to discharge in the evaluation phase, for example, if output is low and we apply inputs which give low output then in pre-charge phase the output will charge to high voltage and during evaluation phase it will discharge to low, increasing the power dissipation. Therefore, the signal activity increases for this circuit design technique and this increased signal activity along with the extra load that the clock line has to derive are the main reasons for high power dissipation in domino logic as compared to static CMOS circuits [5]. Noise margin of Domino logic circuits is low as compared to static CMOS circuits so they are not as scalable as static CMOS. So transistor threshold voltage is kept high to reduce leakage in domino logic circuits. As compared to static CMOS area is reduced in domino logic circuits because of the reduced number of PMOS transistors.

B. Foot Less Domino Logic(FLDL)

Footless domino logic circuit is a standard domino logic circuit shown in Fig.2. Employing a PMOS keeper transistor to reduce charge sharing problem.

C. High Speed Domino Logic

The circuit of the HS Domino logic is shown in Fig.3 [7]. In HS domino the keeper transistor is driven by a combination of the output node and a delayed clock. The circuit works as follows: At the start of the evaluation phase, when clock is high, MP3 turns on and then the keeper transistor MP2 turns OFF. In this way, the contention between evaluation network and keeper transistor is reduced by turning off the keeper transistor at the beginning of evaluation mode. After the delay equals the delay of two inverters, transistor MP3 turns off. At this moment, if the dynamic node has been discharged to [8] ground, i.e. if any input goes high, the nMOS transistor MN1 remains OFF. Thus the voltage at the gate of the keeper goes to VDD-Vth and not VDD causing higher leakage current though the keeper transistor [8]. On the other hand, if the dynamic node remains high during the evaluation phase (all inputs at 0, standby mode); MN1 turns on and pulls the gate of the keeper transistor. Thus keeper transistor will turn on to keep the dynamic node high, fighting the effects of leakage.

Fig. 2. Foot Less Domino Logic [6]

Fig. 3. High Speed Domino Logic [8]
III. PROPOSED DOMINO LOGIC SCHEME

The Proposed circuit is shown in figure 4. Here in this two extra PMOS transistor M3 and M4 has been used in the pull down network. Because of the stacking of these two PMOS transistor in Pull Down network a voltage drop occurs in across it. There is an NMOS transistor in parallel of PMOS stack in pull down network which is sometimes called evaluation transistor. Therefore when the pull down network is in standby mode this PMOS stack reduces the leakage current which directly reduces the leakage power consumption of the circuit. The overall power consumption of the circuit is also reduces by using this technique. The modified design uses a stack of PMOS transistor has been added in the footer circuit standard domino logic. the schematic and configuration of this approach work in a manner so it can reduce the leakage to ground and indirectly reduces the power dissipation novel low-leakage-power design is described.

Fig. 4. Proposed Domino Logic Circuit

The transistors are held in reverse body bias. This reverse body biasing increases their threshold. This increased threshold voltage results in low leakage current and hence low leakage power. As we know the leakage current is the main cause of power dissipation we have reduce the leakage power using a stack of PMOS transistor in Footer circuits. PMOS degrades the low logic level. As we know that static power is relative to the voltage apply, through the reduced voltage the power decreases and we get the advantage of less degradation of logic. This approach contains another advantage during off mode if we increase the threshold voltage PMOS Transistors in Footer Circuits. The transistors are held in reverse body bias. Because as result their threshold is high, higher threshold voltage causes low leakage current and therefore low leakage power. If we use minimum size of transistors, i.e. aspect ratio of 1, we yet again get low leakage power due to low leakage current. As a result of stacking, PMOS footer transistor will get less drain voltage. The output behavior of the proposed Domino logic verified using the simulation of the proposed circuit for OR gate logic. Output is evaluated in the evaluation phase when the CLK=1.

IV. SIMULATION AND COMPARISON

The circuit is simulated using IBM 90 nm and 45nm CMOS technology using 1V. The circuit is simulated for OR gate logic to know its behavior in pull down network and it was found the proposed circuit performs better than the previous techniques. Further in figure 5 and 6 and 7 the output waveform of the Previous and Proposed work.

Fig. 5. Previous Work Output Waveform[9]

Fig. 6. Proposed Domino logic output waveform at 90nm
Table 1 shows the power and delay of the modified circuit in comparison to the previous work. To see the current designer performance for different CMOS technology the modified circuit has been simulated on 90 nm and 45 nm CMOS technology.

Table 1: Power and Delay comparison proposed circuit in 45nm and 90nm CMOS technology

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<th>Circuit Type</th>
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<th>45nm</th>
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<td>Power(W)</td>
<td>9.756E-009</td>
<td>6.306E-010</td>
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<tr>
<td>Delay(s)</td>
<td>8.927E-010</td>
<td>4.186E-010</td>
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Table 2: Power and Delay comparison of the modified circuit with the previous work

<table>
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Table 2 clearly shows the modified circuit performs better on 45 nm CMOS technology. In the modified design there has been used two PMOS transistor in footer circuit. The effect of these transistor analyzed using the individual simulation of these two PMOS transistor in increasing as well as decreasing W/L ration.

V. CONCLUSION

In this work, there has been proposed a high performance low power domino logic Circuit. This circuit have low power as well as high speed hence it achieves the less power delay product. The modified circuit shows high durability on both the 45nm and 90nm CMOS technology plate forms. This circuit can perform well with different design of dynamic logic.

References


