Design and Implementation of 3-Phase 3-Level T-type Inverter with Different PWM Techniques

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Abstract—Multi-level inverter has a capability to handled high power with less total harmonic distortion (THD), reduced switching losses and good power quality due to which in recent year they become more popular in high power application, with Increase in the voltage level, harmonic content in output waveform will decrease. Diode Clamped Multilevel Inverter (DCMLI) has a capability to increase the output voltage and performance with low switching losses, reduced voltage stress and total harmonic distortion. However, it suffers from problems of high conduction losses. T-type is used to overcome the drawbacks of DCMLI, but the high side and low side power devices of T-type inverter need to block the whole dc link voltage. The switching frequency is limited due to the high switching losses caused by the high voltage rated power devices. Generally, it is used for both low conduction losses and switching losses with high switching frequency. Simulation result of 3-phase 3-level T-type multi-level inverter can be obtained by MATLAB/ SIMULINK software multi-level inverter using different PWM technique.

Keywords- Multi-level inverter(MLI); DCMLI; T-type inverter; SPWM and ISPWM techniques.

I. INTRODUCTION

An inverter is used to convert dc to ac power at a desired ac voltage. But a multilevel inverter can generate a stair-case voltage waveform with less distortion, less switching frequency and higher efficiency. While conventional inverter having two voltage level is commonly used for domestic and commercial applications, since its configuration is simple and the reliability is better. However, there is a some limitations in high power and performance due to two level inverter output voltage is depend on Vdc. The basic idea of MLI is that the dc link voltage can be split between different power switches, which can provide intermediate voltage levels between the reference potential and the dc link voltage. Multilevel inverter provides many advantages over two-level inverter, it increase the output voltage waveform, reduced EMI and (dv/dt) voltage stress on the load, lower switching frequency and low rating devices for high power rating, but the copper loss, torque ripple and higher number of semiconductor switches are increased because of low frequency harmonics. Every switch requires a separate gate driver circuit, therefore increasing the complexity and size of the overall circuit. The SPWM strategy is commonly used to solve the harmonic problem of this six-step method in many applications. The switching loss is more prominent when the switching frequency is increased and the DC link voltage becomes higher. Therefore a three-level inverter is being researched in various applications for further improvement of energy efficiency, reliability, power and density.

The multilevel inverter topology such as the three-level inverter has been developed for both medium and high voltage level. Among various conventional multilevel inverter are categorized as Diode Clamped Multilevel Inverter (DCMLI) [1], Flying Capacitor multilevel inverter (FCMLI) [2] and Cascaded H-bridge multilevel inverter (CHBMLI) [3] have been widely used. In 1981 Nabae introduced a three level diode clamped inverter schemes,[4-5] research on the conventional DCMLI applied in the renewable energy system. The clamping diodes in [4-5] are replaced by the IGBTs to reach active clamping in [6] to improve the semiconductor loss distribution[7] proposes a novel high efficiency stacked neutral point clamped 3L-NPC inverter[8] proposes an active clamped 3L-SNPC to improve the 3L-SNPC’s structure and control strategy are improved the 3L-SNPC’s efficiency[9] the 3L-SNPC’s structure and control strategy are improved to reduce the power loss, specifically in the low power range. The DCMLI having the switching loss in each switch is
half and the conduction losses become double of the counterpart of the two-level inverter due to the two switch series connection.

This paper proposes a 3-level T-type inverter topology which requires less number of switches and gate driver circuits as compared to conventional multilevel inverters. The T-type topology that was previously proposed here is implemented in three-phase with different PWM techniques. The pulse-width modulation (PWM) control is the most efficient method of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. The paper tries to prove that 3LTI is better than conventional multilevel inverters in terms of their number of components and THD. Even though the 3LTI is generally implemented and investigated to apply in low-voltage applications, it has difficulties to apply in low-voltage and low-power domestic appliances because the increased efficiency is not sufficient due to its complexity and cost problem.

First of all, the long current paths imply the high conduction loss. Second, higher stray inductance due to the long current paths results in higher power loss and turn-off overvoltage. To overcome these characteristics in the multi-level topology, the 3-Level T-type inverter (3LTI ) has been proposed for the high efficiency and performance in low-voltage applications.

II. T-TYPE MULTILEVEL INVERTER

The basic topology of the 3-Level T-type is depicted in Fig. 2.1 [10]. The conventional two-level VSI topology is extended with an active, bidirectional switch to the dc-link midpoint. For low-voltage applications, the high side and the low-side power switches (T1 and T4) would usually be implemented with IGBTs as the full dc-link voltage has to be blocked. The block dc link voltage is twice of the DCMLI inverter. When both IGBTs connected in series turn off at the same time. This undesirable effect cannot occur in the T-type topology. A 3-Phase 3-Level T-type inverter is implement low-level routines which prevent such transitions or ensure a transient voltage balancing among series connected IGBTs. [11] applies 3L T-type in the solar system to avoid the high conduction loss.

Cascaded multilevel inverter reaches higher reliability. The cascaded inverter is used for large automotive electric drives. However, the requirement of more number of switches and separate dc source for each cell becomes a problem especially at higher level. The pulse-width modulation (PWM) control is the most efficient method of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. The paper tries to prove that optimization method is better than conventional multilevel inverters in terms of their number of components and THD.

First of all, the long current paths imply the high conduction loss. Second, higher stray inductance due to the long current paths results in higher power loss and turn-off overvoltage. It should be mentioned that the foregoing discussed drawbacks of DCMLI seem more prominent in renewable energy system because they are usually operating in much lower power range than the rated power.
There are basically two ways; the two IGBTs can be configured to form a bidirectional switch, either in common emitter configuration or common collector configuration. The common emitter configuration as in Fig. 2.1 (T2 and T3) would require one additional isolated gate drive supply voltage for each bridge leg, summing up to three additional gate drive supplies compared to the two-level VSC topology. T1 shares now a common emitter with the high-side switch T1 and can supplied with the isolated gate drive voltage of T1 and can be supplied with the isolated gate drive voltage of T1. The emitter of the second IGBT is connected to the midpoint voltage level. If the 3-phase topology is considered, all three IGBTs share a common emitter, and therefore only one isolated gate drive supply is necessary. In total, the complete T-type topology can be implemented with only one additional isolated gate drive supply compared to the two-level topology.

### III. MODES & OPERATION

#### Mode – I

*Fig. (a). Level 1 (+Vdc/2 volt)*

#### Mode – II

*Fig. (b). Level 0 (0 volt)*
TABLE-I (SWITCHING TABLE)

<table>
<thead>
<tr>
<th>Generation of Level</th>
<th>Switching Devices</th>
<th>Output Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>+Vdc/2</td>
<td>on off On off</td>
<td>+1v</td>
</tr>
<tr>
<td>0</td>
<td>off on On off</td>
<td>0v</td>
</tr>
<tr>
<td>-Vdc/2</td>
<td>off on Off on</td>
<td>-1v</td>
</tr>
</tbody>
</table>

The necessary power rating of the isolated gate drive supply of the high-side switch T1 is not increased if the gate charges of the IGBT are approximately equal. Because of the implemented commutation and modulation strategy T1 and T2 are newer switched both in the same modulation cycle. Operation of the one leg of 3-Phase 3-level T-type inverter with can be easily explained with the help of Fig. 3 and table I. When switches T1 and T3 are turned “on” the output voltage will be “+Vdc/2” (i.e., level 1). When switches T2 and T3 are turned “on” the output voltage is zero (i.e., level 0). When switches T2 and T4 are turned “on” the output voltage will be “-Vdc/2” (i.e., level -1).

The operation of this topology can also be easily understood by mode of operation of Single-phase 3-level T-type NPC shown in Fig.3. The voltage source “Vdc” is required 100V. There are three sufficient switching modes in generating the multistep level for a 3-level T-type inverter.

IV. MODULATION TECHNIQUES

There are different pulse width modulation strategies with different phase relationships;

- Phase disposition pulse width modulation (PD PWM):- In phase disposition pulse width modulation strategy, where all carrier waveforms are in same phase shown in fig. 4(a).

![Carrier arrangement for PDPWM strategy](image-url)
• Phase opposition disposition pulse width modulation (POD PWM):- In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are 180° out of phase Shown in fig. 4(b).

Fig. 4(b). Carrier arrangement for PODPWM strategy

• Alternate phase opposition disposition pulse width modulation (AOD PWM):- In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier by 180°. Shown in fig. 4(c).

Fig. 4(c). Carrier arrangement for AODPWM strategy

• Inverted Sine Carrier PWM (ISCPWM):- This control strategy replaces the conventional triangular based carrier waveform by inverted sine wave which has a better spectral quality and a higher fundamental output voltage without any pulse dropping[11]. This technique combines the advantage of inverted sine and constant or variable frequency carrier signals as shown in Fig. 3.12 and Fig. 3.13 respectively. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been shown [12]-[13]. Both the techniques are explained in brief.

Fig. 4(d). Carrier arrangement for ISCPWM strategy
• Variable Frequency Inverted Sine Carrier PWM (VFISCPWM): The VFISCPWM technique provides an enhanced fundamental voltage, lower THD and minimizes the switch utilization among the bridges in inverters [14]. The number of active switching among the bridges is balanced by varying the carrier frequency based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all bridges.

![Carrier arrangement for VFISCPWM strategy](image)

**Fig. 4(e). Carrier arrangement for VFISCPWM strategy**

V. SIMULATION RESULTS

The simulation parameters are as following: dc source voltage is 100V; Frequency of carrier signal is 4 kHz. In this paper, three PWM techniques are used PD, POD, and APOD, with same modulation index (Ma). For Ma = 1.0, and Mf = 20, corresponding (%) THD are PD = 84.62%, POD = 71.55%, APOD = 71.55%, ISCPWM = 98.49% and VFISCPWM = 95.96%. Based on the PWM techniques, the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

![Carrier Modulation Signals of Three-Phase 3-Level T-type.](image)

**Fig. 5.1: Carrier Modulation Signals of Three-Phase 3-Level T-type.**
Fig. 5.2: Simulated Three-Phase Voltage by PDPWM for R-Load.

Fig. 5.3: Phase output voltage by PD (Ma=1.0, Mf=20).

Fig. 5.4: Phase output voltage by PODPWM (Ma=1.0, Mf=20).
Fig. 5.5: Phase output voltage by APODPWM (Ma=1.0, Mf=20).

Fig. 5.5: Phase output voltage by ISCPWM (Ma=1.0, Mf=20).

Fig. 5.5: Phase output voltage by VFISCPWM (Ma=1.0, Mf=20).
TABLE-II (NUMBER OF COMPONENTS)

<table>
<thead>
<tr>
<th>Inverter Type</th>
<th>DCMLI</th>
<th>FCMLI</th>
<th>CHBMLI</th>
<th>T-Type NPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Switches</td>
<td>04</td>
<td>04</td>
<td>04</td>
<td>04</td>
</tr>
<tr>
<td>Main Diodes</td>
<td>04</td>
<td>04</td>
<td>04</td>
<td>04</td>
</tr>
<tr>
<td>Clamping Diodes</td>
<td>02</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>DC Bus Cap/Isolated Supplies</td>
<td>02</td>
<td>02</td>
<td>0</td>
<td>02</td>
</tr>
<tr>
<td>Flying Capacitor</td>
<td>0</td>
<td>03</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Total Numbers</td>
<td>12</td>
<td>13</td>
<td>08</td>
<td>10</td>
</tr>
</tbody>
</table>

TABLE-III (TOTAL HARMONIC DISTORTION)

<table>
<thead>
<tr>
<th>Modulation Index</th>
<th>PDPWM</th>
<th>PODPWM</th>
<th>APODPWM</th>
<th>ISCPWM</th>
<th>VISCPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>84.62%</td>
<td>71.55%</td>
<td>71.55%</td>
<td>98.49%</td>
<td>79.80%</td>
</tr>
<tr>
<td>0.9</td>
<td>105.84%</td>
<td>84.10%</td>
<td>84.10%</td>
<td>129.49%</td>
<td>95.96%</td>
</tr>
<tr>
<td>0.8</td>
<td>170.19%</td>
<td>91.74%</td>
<td>91.74%</td>
<td>187.64%</td>
<td>115.59%</td>
</tr>
</tbody>
</table>

Fig. (a) Total Harmonic Distortion of T-type inverter

VI. CONCLUSION

In this paper, a 3-level T-type inverter is proposed with different PWM techniques used to generate 3-level output phase voltage. It is proved that the proposed work of 3-Phase 3-Level T-type inverter output voltage total harmonics distortion is reduced and improve the efficiency of system compared with different PWM techniques. Harmonic analysis carried out using Mat Lab R2009a version software. Simulation results show the performance of 3-Phase 3-Level T-type inverter with different PWM techniques. Table-II shows the number of power switches [IGBTs] and output voltage steps in the proposed topology. This proposed MLI topology requires less number of components as compared to conventional MLI inverters.

REFERENCES


