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Design of a High Gain 2.4-GHz Differential Low Noise Amplifier using TSMC 180nm Technology

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ABSTRACT

A differential input differential output low noise amplifier is designed here. The designing is done using 180nm CMOS RF process. The LNA operates at 2.4-GHz frequency. This paper presents the LNA with cascode topology using inductive degenerated common- source CMOS LNA in order to provide the improved gain, linearity and better isolation. The simulation and analysis is performed using Cadence Virtuoso IC tool. This design exhibits a gain of 18.25 dB, input return loss (S_{11}) of -7.45 dB, isolation (S_{12}) of -32.2 dB and minimum Noise Figure of 1.3 dB. The circuit operates at supply voltage of 1.8V.

Keywords

Cascode topology, Noise Figure, low noise amplifier (LNA), radio frequency (RF).

INTRODUCTION

The increasing demand of wireless applications such as mobile phones, WLANs, remote receivers encourage us to go for the circuits which provide optimization. RF integrated circuits always seek for optimization as there are some challenges in the designing of the circuits which can provide minimum power consumption as well as high speed and low noise.

The LNA is typically the first stage of an RF receiver. Its main function is to provide enough gain to overcome the noise of subsequent stages. Moreover, it should show a specific impedance, such as 50 Ohm, to the input source[1]. There are a lot of trade offs in the designing of LNA with several topologies. The ultimate goal is to achieve a device with high performance and low noise. For this purpose, this paper presents a cascoded CMOS LNA with differential input and differential output. The single-ended architecture is sensitive to parasitic ground inductance while the differential architecture is able to reject common-mode disturbances.

DESIGN METHODOLOGY

Although the single-ended input architecture is capable of consuming very less power and the area occupied is also very less. We use differential-ended input architecture which consumes almost double power, since its ability to improve noise and linearity performance. It cancels the even-order harmonics thus improves the linearity.

A typical differential amplifier is shown in figure-1. The inductor degeneration topology provides the control over the real part of the input impedance without allowing the actual resistors noise in the circuit. The cascoding improves the input-output isolation as there is no direct coupling from output to input.

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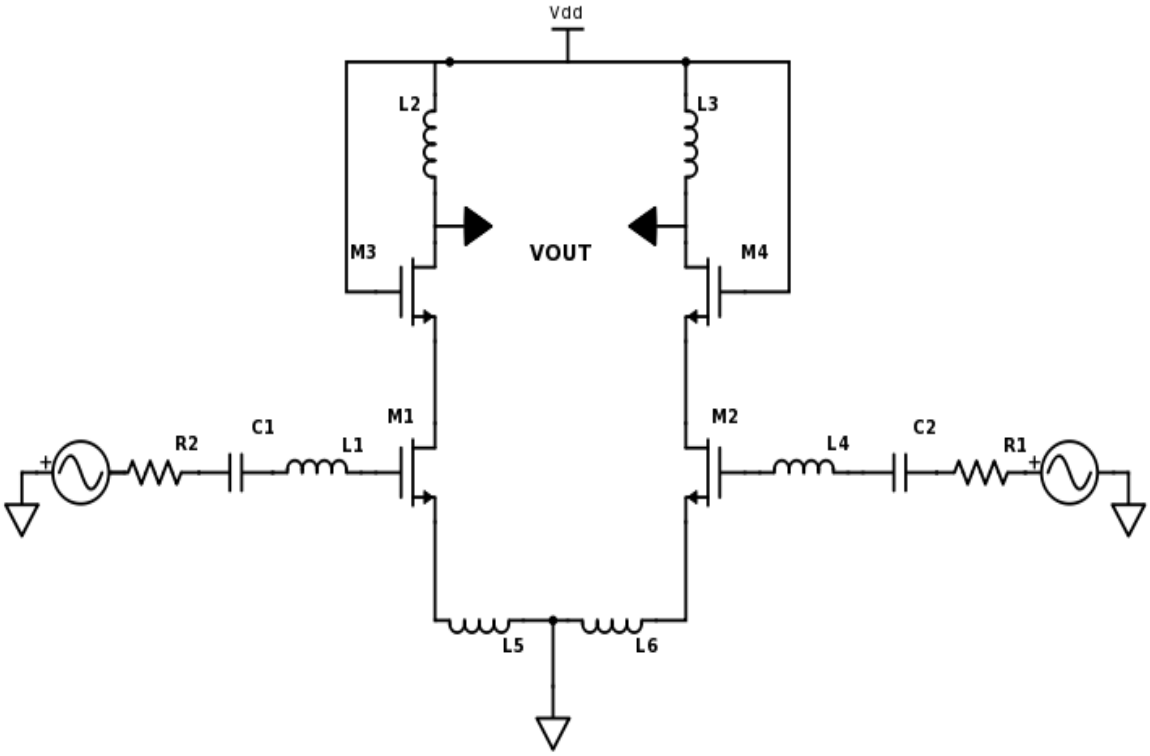

Fig 1: Typical Differential Amplifier

PROPOSED LNA DESIGN

M1 and M2 are the main transistors, M3 and M4 are the cascoding transistors. Additional circuitry is used in the circuit for the proper biasing.

To obtain the optimized width of M1, we use the power constrained noise minimization technique.

$$\textbf{Wopt} = \frac{1}{3wCoxLRs}$$

Here, Wopt is the optimized width of transistor M1. L is the effective channel length of transistor. Cox is the oxide capacitance. Rs is the input source resistance which is equal to 50 Ohm here.

Wopt helps to determine the gate-to-source capacitance Cgs of transistor M1. It can be calculated as;

$$Cgs = \frac{2WoptCoxL}{3}$$

The proper value of source degenerated inductor 'Ls' can be obtained as

$$Z = jwLs + \frac{g_m Ls}{Cgs} + \frac{1}{jwCgs}$$

The individual inductance and capacitance part would be resonated out and remaining part should be equal to 50 Ohm.

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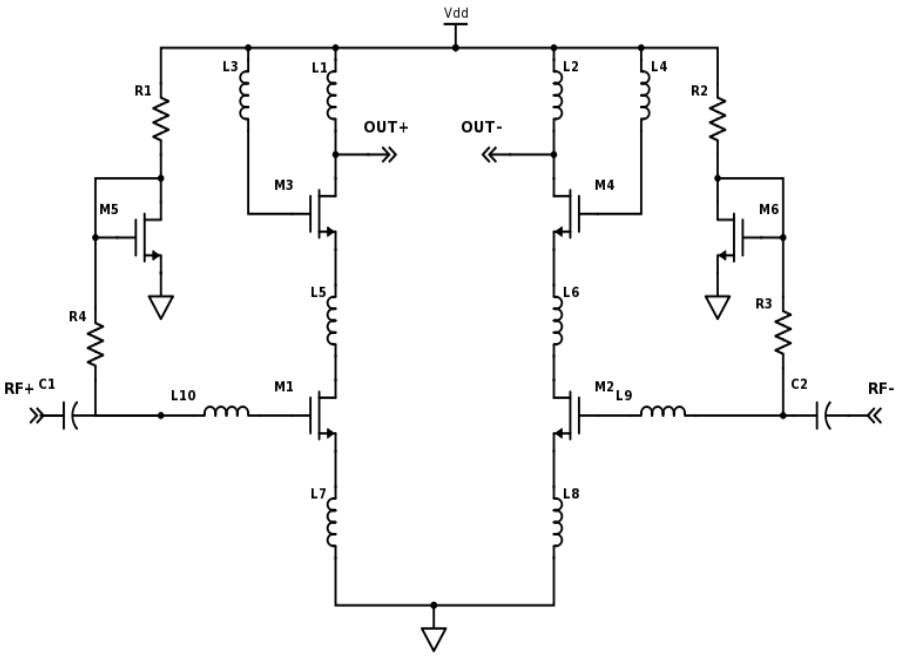

Fig 2: Proposed differential LNA

Figure-2 represents the proposed differential input differential output LNA circuit. The optimum value obtained of Wopt after calculation is 290um. In order to maintain symmetry, width of M1, M2, M3 and M4 are kept to be the same. The width of M5 is kept one tenth of M1 so as to provide the proper biasing current.

The gate inductor L10 at the gate of M1 is approximately 15nH and the degenerated inductor L7 is 144pH. L5 and L3 are used for the proper biasing. The supply voltage applied is 1.8 V.

SIMULATION RESULTS

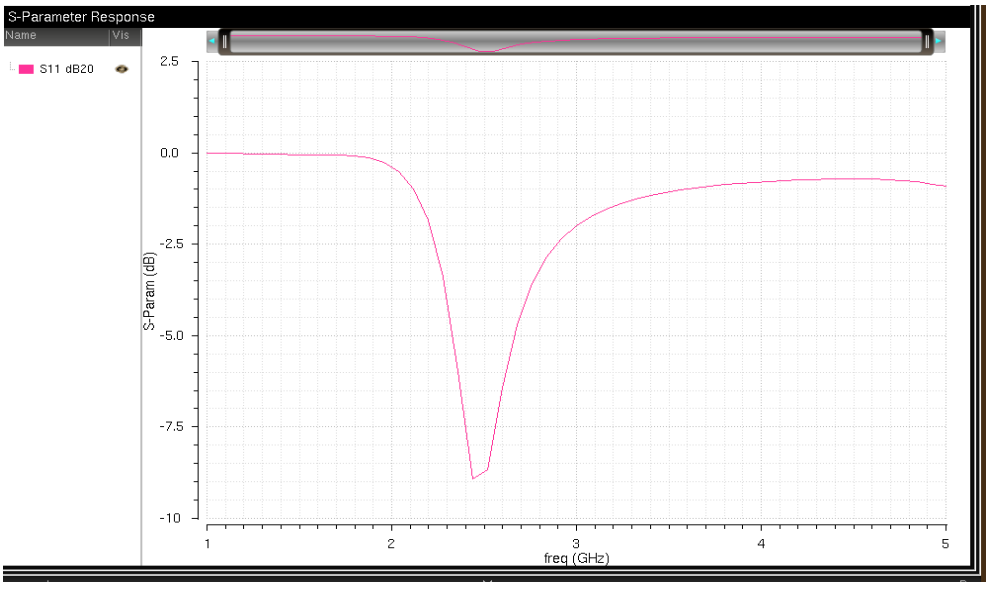

Fig 3

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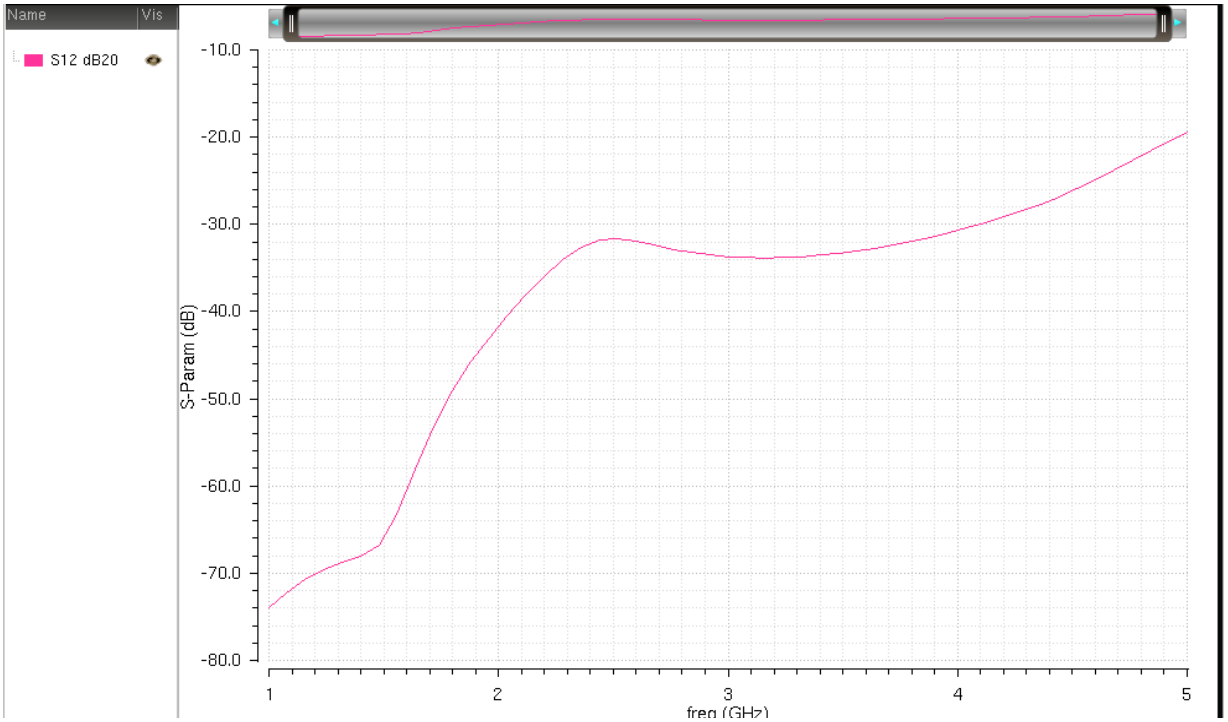

Fig 4

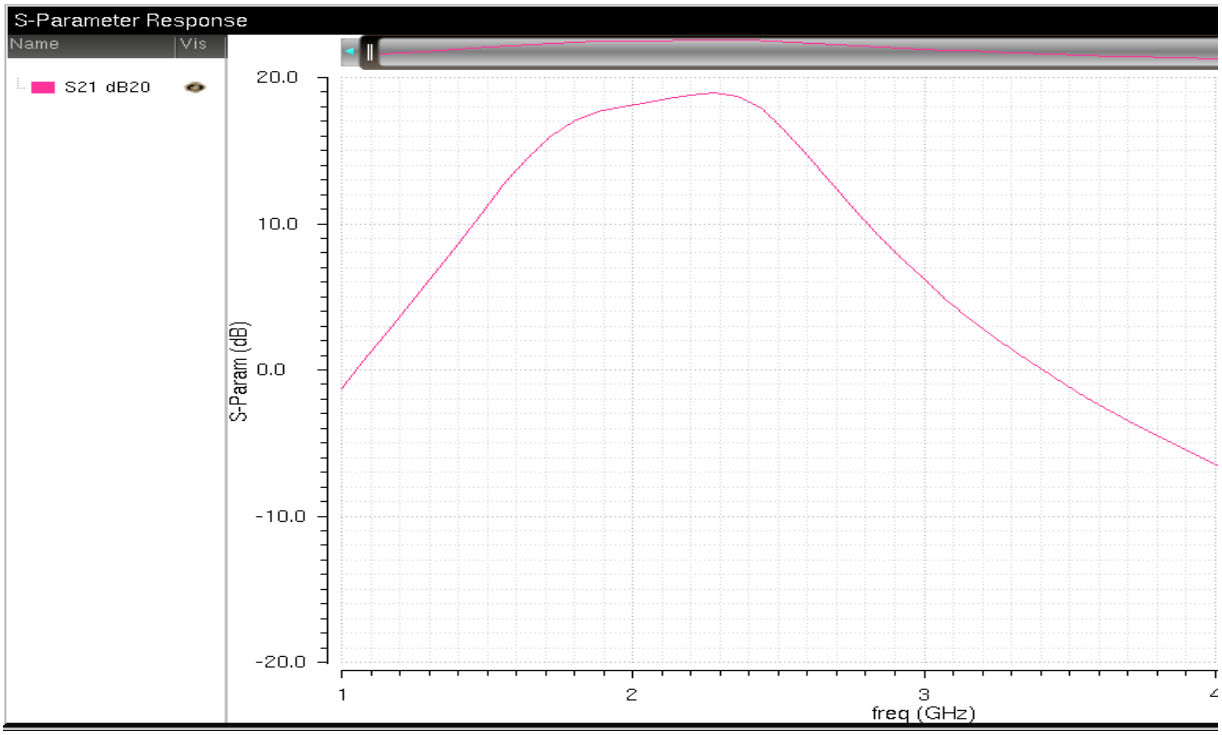

Fig 5

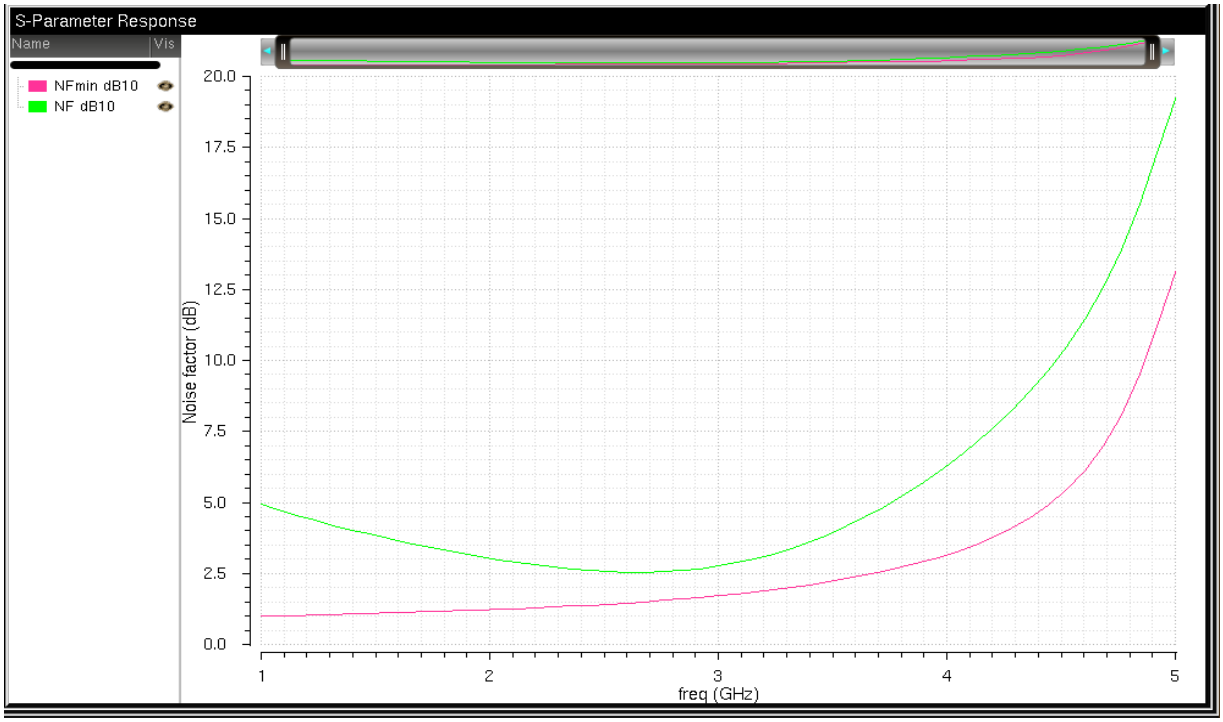

Fig 6

Table 1. Simulation results

Parameters	This works
Frequency	2.4-GHz
CMOS Process (um)	0.18
NFmin (dB)	1.3
NF (dB)	2.6
Supply Voltage (V)	1.8
Power gain S21 (dB)	18.25
Reverse Isolation S12 (dB)	-32.2
Input return Loss S11 (dB)	-7.45

The proposed LNA is designed using 180nm CMOS RF process. The simulation was performed on Cadence Virtuoso tool. The LNA operates at 2.4 GHz frequency. Fig. 3-6 represents the S-parameters and Noise figure results obtained during simulation of the proposed circuit.

CONCLUSION

The simulation results shows that the proposed differential LNA exhibits very high gain and low noise figure. The results are being obtained by simulating the circuit at 2.4 GHz frequency using 0.18um CMOS technology. The reverse isolation is also very high as desired. The supply voltage used during the simulation is 1.8 V.

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