International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 6
June 2017

Power Reduction through Different Low Power CMOS Technique in Power Gating Switch

Anuj Agrawal , Honey Kumar
Department of Electronics & Communication Engineering
Hindustan College of Science & Technology, Farah , Mathura,

ABSTRACT

In this thesis has introduced two new techniques for low CMOS switch circuit design techniques as Lector technique and Galeor technique for reducing the leakage power dissipation in CMOS switch circuit. low power CMOS switchs are performance depends on these two techniques reduce the leakage power dissipation. These technique are implemented in the CADENCE virtuoso tool to find the leakage power dissipation and propagation delay. This proposed Lector and Galeor techniques are proved better leakage power reduction than the MTCMOS techniques. This work presented a lector based CMOS switch and Galeor based techniques. Thus the Lector and Galeor techniques are used in the low power switch design enabling three different modes: active, drowsy, and sleep. Leakage power reduction in the mode transition is reducing to comparing with MTCMOS. We analysed that the propagation delay of these technique is lesser than the MTCMOS technique. The lector technique have lower leakage power dissipation than the other low power switch technique.

Keywords: -MTCMOS, leakage power, sleep transistor

1. INTRODUCTION

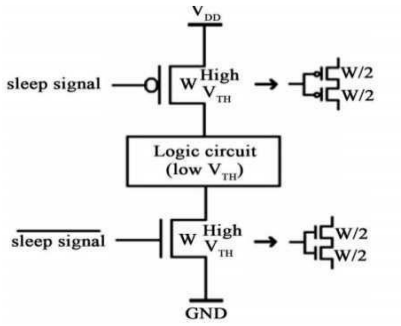
In the last some years due to the ever growing demand for portable and small sized devices, integrated circuits need electronic circuit design methods to implement integrated circuits with low power consumption. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent years has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the system.If we want a design and implement for low-power consumption to be successful, it is important to have a complete knowledge of the sources of power dissipation, the reasons that affect them, and the methodologies and techniques that are available to get optimal results. Therefore, this paper starts with the sources of leakage power in a integrated circuit. we believe in the most important low-power methodologies and power optimization techniques available. Apart from that, also a number of alternative logic design styles are presented to report on their characteristics regarding power consumption. This Paper could be utilized by others as a quick study in the field of power-aware design. So we are designing the Switch using four different technique to find low power dissipation and lesser delay by comparing these four different technique.

2. Regular Four Technique

2.1 Partial Stacking

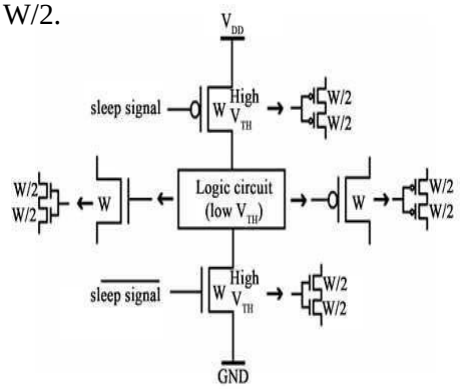
The proposed logic circuit for hybrid MTCMOS partial stack technique is shown. In this technique, a high VTH PMOS transistor (sleep PMOS transistor) is inserted between VDD and the pull up network and a high VTH NMOS transistor (sleep NMOS transistor) is inserted between the pull down network and GND. Then stacking of only high VTH sleep PMOS and high VTH sleep NMOS transistors are done. In this technique, stacking of low VTH NMOS and PMOS transistors of the logic circuit is not performed. Here, only partial stacking of high VTH sleep PMOS and sleep NMOS transistors are done to reduce the overall circuit propagation delay in active mode.

International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 6
June 2017



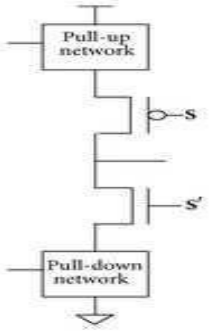
2.2 Complete Stacking

The proposed logic circuit for hybrid MTCMOS complete stack technique is shown in Fig .In this technique, a high threshold voltage PMOS transistor (sleep PMOS transistor) is inserted between VDD and the pull up network and a high threshold voltage NMOS transistor (sleep NMOS transistor) is inserted between the pull down network and GND. Then stacking of all transistors (high VTH sleep PMOS, high VTH sleep NMOS and low VTH transistors of the logic circuit) are done by replacing each transistor of width W with two series connected transistors of width W/2.



2.3 Galeor Technique

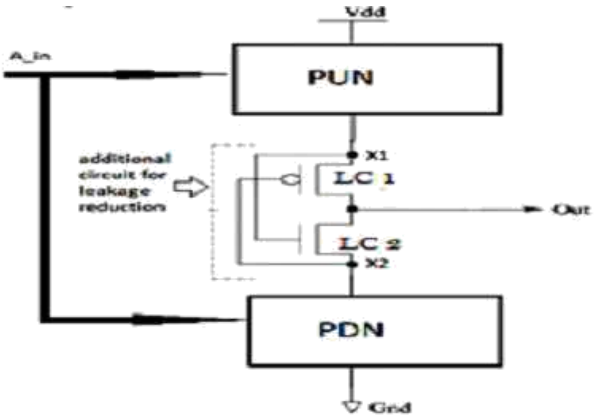
In this technique two gated leakage transistors are inserted between pull-up and pull-down networks of CMOS circuit. Gated leakage NMOS transistor is placed between output and pull-up circuit and a gated leakage PMOS transistor is placed between output and pull-down circuitry. The gates of these additional transistors are con-trolled by the drain voltages. Gated Leakage transistors cause increase in resistance of the path from Vdd to ground since one of the leakage transistors is always near its cut off region, hence decreasing leakage current. This technique can also be implemented in larger circuits like memory elements by placing gated leakage transistorsat the output gates. Gated leakage transistors must have threshold voltage higher than the transistors used in pull up and pull down network.



International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 6
June 2017

2.4 Lector Technique

In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence static power dissipation. We propose a novel technique called LECTOR for designing CMOS gates which significantly cuts down the leakage current without increasing the dynamic power dissipation. In the proposed technique, we introduce two leakage control transistors (a p-type and a n-type) with in the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other.



3. Proposed Method

3.1 Switch Using Partial Stacking

The two serially connected devices in the off state have significantly lower leakage current than a single off device. This is called the stacking effect. With transistor stacking by replacing one single o transistor with a stack of serially connected off transistors, leakage can be significantly reduced.

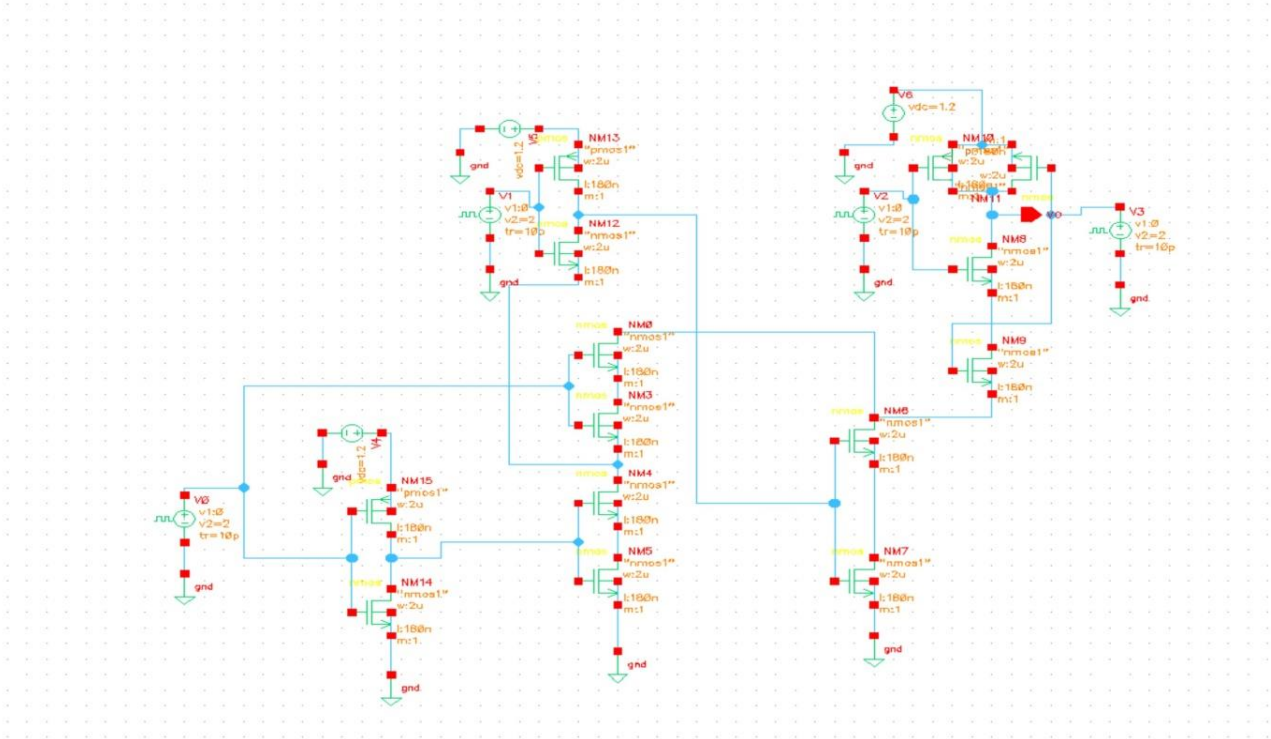


Figure 3.1: schematic of Switch Using Partial Stacking

International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 6
June 2017

3.2 Switch Using Complete Stacking

This is a State destructive technique which cuts off either pull-up or pull down or both the networks from supply voltage or ground or both using sleep transistors.

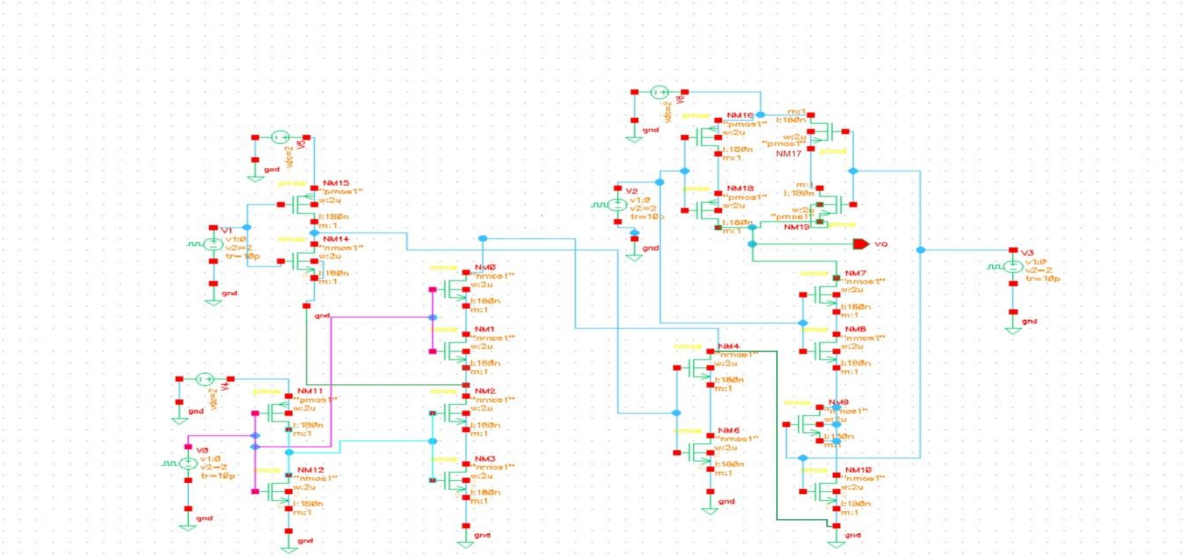


Figure 3.2: schematic of Switch Using Complete Stacking

3.3 Switch Using Lector Technique

In lector technique two leakage control transistors (a p-type and an n-type) are introduced within the logic gate for which the gate one of the LCTs is always near its cut-off voltage for any input combination. This increases the resistance of terminal of each leakage control transistor (LCT) is controlled by the source of the other.

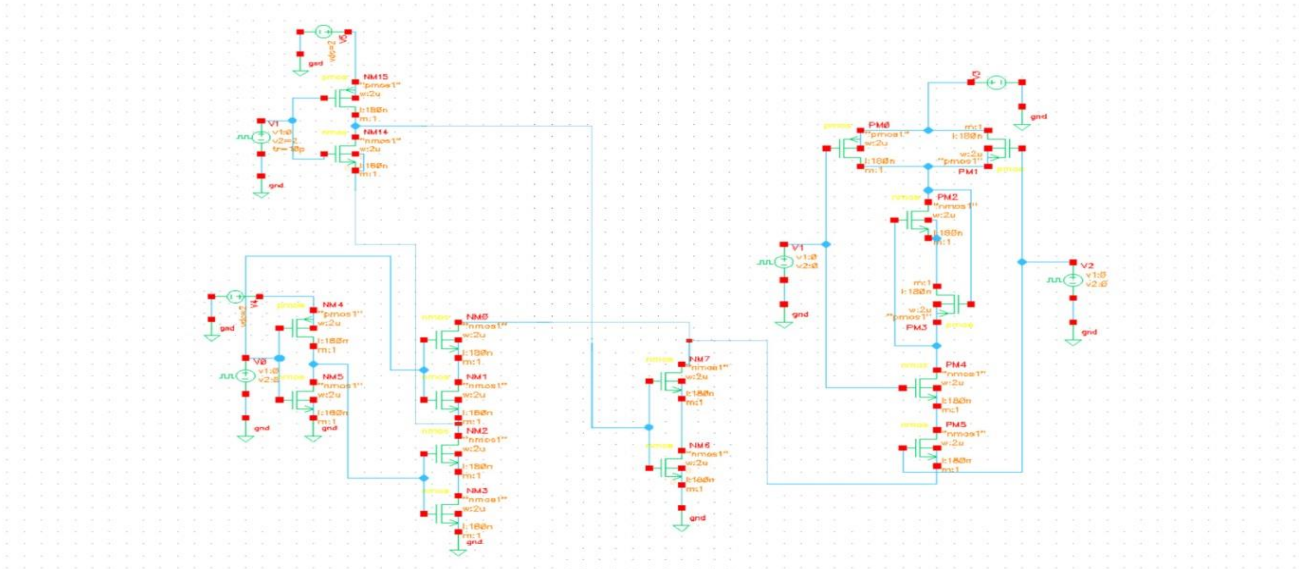


Figure 3.3: schematic of Switch Using Lector Technique

3.4 Switch Using Galeor Technique

In the Galeor technique two gated leakage transistors are inserted between pull-up and pull-down networks of CMOS circuit. Gated leakage NMOS transistor is placed between output and pull-up circuit and a gated leakage PMOS transistor is placed between output and pull- down circuitry.

International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 6
June 2017

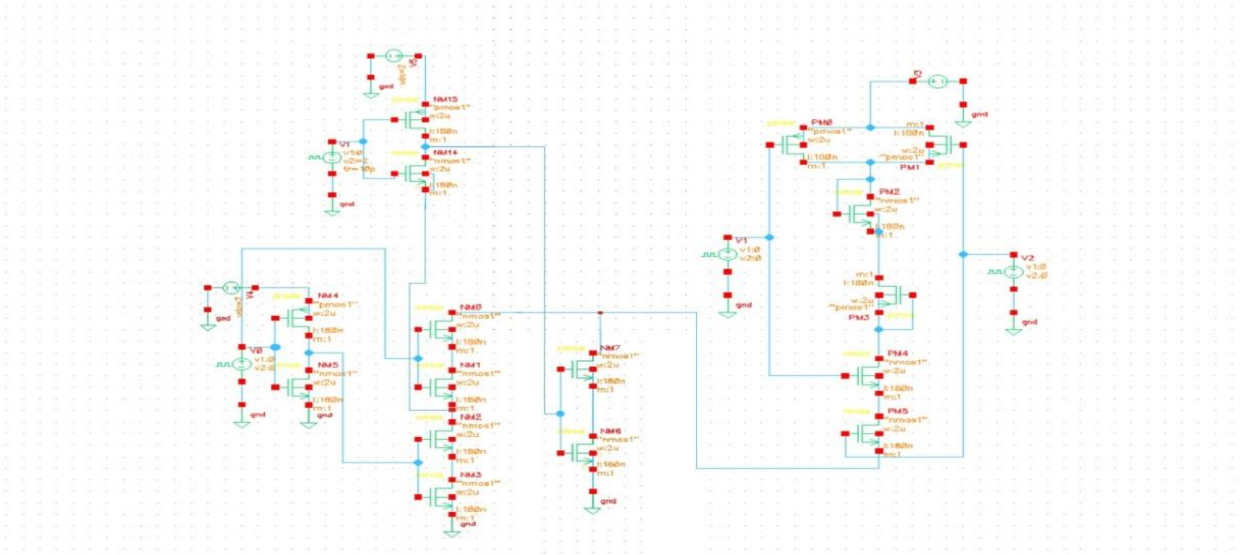


Figure 3.4: schematic of Switch Using Galeor Technique

4. Results and Simulation

Table 4.1: Comparison of all Techniques in 180nm Technology

180nm Technology		
Technique	Power	Delay
Partial Stacking	185.2E-6	190.7E-12
Complete Stacking	231.6E-6	238.3E-12
Lector	46.30E-6	95.34E-12
Galeor	92.59E-6	143.0E-12

5. Conclusion

In this work two new low power techniques are used to design as Lector technique and Galeor technique for reducing the leakage power dissipation in mode transition. low power switch are performance depends on these two techniques reduce the leakage power dissipation. These technique are implemented in the CADENCE virtuoso tool to find the leakage power dissipation and propagation delay. This Proposed Techniques (Lector Technique) are proved better leakage power reduction and delay than the Partial Stacking, Complete Stacking and Galeor Techniques. A Switch has been designed using these techniques and power dissipation is calculated and is compared with MT CMOS technique. Simulation results show the validity of the proposed techniques is effective to save power dissipation and to increase the speed of operation of the circuits to a large extent.

6. REFERENCES

1. Ehsan Pakbaznia and Massoud Pedram, Design of a Tri-Modal Multi- Thresh-old CMOS switch with application to to Data Retentive Power Gating, IEEE transactions on vlsi systems., vol. 20, no. 2, February 2012,pp.380385.
2. K. Agarwal, H. Deogun, K. Nowka, D. Sylvester, Power Gating With Multiple Sleep Modes, in Proc. Int. Symp. Quality Electron. Des., 2006, pp. 633637.
3. Johnson M, Somasekhar D, Chiou L-Y, et al. Leakage control with efficient use of transistor stacks in single threshold CMOS. IEEE Trans. Very Large Scale Integration. (VLSI) Syst. 15 Feb 2002; 10(1).
4. Kang S. Accurate simulation of power dissipation in VLSI circuits. IEEE Jour-nal of Solid-State Circuits. 1986; 88991p
5. T. Austin, S. Das, D. Blaauw, and S. Lee, T. Mudge, T. Pham, Reducing Pipeline Energy Demands with Local DVS and Dynamic Retiming, in Proc. Int. Symp. Low Power Electron. Des., 2004, pp. 319324.