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Design of Mixed Radix CORDIC FFT Algorithm

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Abstract*—This electronicrecordportraysthe technique forusageofFastFourier transform for wireless communication systems, like OFDM, digital video broadcasting, digital audio broadcasting,andworldwideinter-operability for microwaveaccess.The highspeedandlowareaFFT algorithmusingCORDICandradix2^5calculation is proposed here. CORDIC is fundamentallyDSP applicationyethereitisutilizedfor twiddle componentaugmentation.Radix2^5fftcalculation isutilizedforlesseningofcomplexduplication. The proposed computationminimizesthe amountof multipliers.Plotoutlines showthattheFFTarranged by theproposedframeworkshowsalowerhardware withmorequality thanexistingsystems.Our designed hasa working frequency up to 420.203 MHZ.CORDICcomputationisexecutedinbothMATLABandinXilinxonVirtex-5.*

Keywords—FFT,IFFT, Radix 2^5, FPGA, CORDICalgorithm

I. INTRODUCTION

1.1 Overview

A Fast Fourier change (FFT) is a quick computationalcalculationtoregister the discrete Fourier change (DFT) and itsconverse. The FastFourierTransform doesnot introducetoanotheror diversesort ofFourier change. It introduce to an extremely productivecalculationforprocessingthe DFT.Thetimetakestoplayouta DFTonaPC dependsfundamentallyonthequantity ofincreases included O (N2)) while FFT just needs Nlog2(N).The focal understanding which prompts this calculation is the acknowledgment that a discreteFourierchangeof an arrangement ofN focusescan becomposed as faras two discrete FourierchangesoflengthN/2.Alongtheselines,if Nisaforceof2,itisconceivabletorecursively applythis deterioration.

Theprimary explorationthoughtofthisworkis advance theconfigurationof FFTprocessor.Areaand power decrease isthe principle targetof thiswork. So CORDIC calculationpresented withradix2^5FFT calculation. The CoordinateRotation Digital Computer (CORDIC)algorithmic, proposed by Jack Voider[1]canbeusedfor abroadcollectionoflimits includingcertain trigonometric,hyperbolic, straight andlogarithmiccapacities.The CoordinateRotation DigitalComputer(CORDIC)algorithmic,proposed by JackVoidercan be utilized for an extensive variety ofcapacitiesincludingcertaintrigonometric, hyperbolic, straightand logarithmic capacities. CORDICunitutilizesjustmoves andaddtofigure these capacities.The CORDICalgorithmprovides an iterativemethodofperformingvectorrotationmode,C ORDICisused forconvertingonevectorin rectangular formto another vector in rectangular form.Inthevectormode,itconvertsa vectorin rectangularformtopolar form.HenceCORDICis usedasanefficientway torealizemultiplication-free FFT[2].Theremainderofthisprojectis organizedas follows:

SectionII andIII reviewtheCORDICalgorithmand the generalhardwarearchitecturesrequiredto implement FFT.

SectionIV introducesthe proposed radixand CORDIC algorithmfor 64 point FFT implementation.

Section V and VI presents the performance evaluation andcomparison andconclusion respectively.

II. REVIEW OFCORDICALGORITHM

The key idea of CORDIC number-crunching dependsonthe basicandoldstandards of two-dimensionalgeometry.Inany case,theiterativeplan ofacomputationalcalculationfor itsexecutionwas

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initially depictedin1959by JackE.Volderforthe calculationoftrigonometric capacities,increaseand division [6][7][9]. CORDICbasedfiguring got expandedattention in1971, when John Walther demonstratedthat, by differingacoupleofbasic parameters,itcouldbeutilizedas asolitary calculationforboundtogetherexecutionof an extensivevariety ofrudimentary supernatural capacities including logarithms, exponentials, andsquare roots alongside those recommended byVolder[7].

CORDICisalluring becauseofthe straightforwardnessof itsequipmentusage,since the sameiterative calculationcouldbe utilizedfor allthe abovenumericalapplicationsutilizing theessential movement include operations of thestructure

x±y2-i.

Theordinary strategy forexecutionofrevolution changeis spoken to bythe conditions.

$$Xout = xin \cos \theta - yin \sin \theta. \quad (1)$$

$$Yout = xin \sin \theta + yin \cos \theta. \quad (2)$$

where(xin,yin)and(xout,yout)arethe underlying and last arranges of thevector separately.

The equipmentacknowledgmentofthese conditions requiresfour increases,two augmentations/subtractionsandgetting tothetable putaway inthememoryfortrigonometric coefficients.The CORDICrotatorperforms2Dturn utilizing aprogressionofparticularincremental revolutionpointschosesothateachisperformedby a movementandinclude operationiteratively.The threebasicequations ofCORDICalgorithm are:

Xi +1=xi– m siyiρ–Sm,i(3) Yi +1=yi + sixi ρ–Sm,i(4) Zi +1=zi-si am, i(5)

Inviewoftheestimationofmthecalculation can work in one ofthreedesigns:

Direct(m=0),Circular(m=1)andHyperbolic(m= -1).Insideeachof these designsthe calculation capacities in one of two modes – pivot or

vectoring.**σ**speaks to either clockwise or counterclockwiseheadingofturn,ρspeakstotheradixof the numberframeworkand the movementgrouping Sm,ireliesonuponthe directionframeworkandthe radixof number framework. Sm,iinfluencesthe joining ofthecalculation.Inturnmode,the informationvectorispivotedby apredetermined point,while invectoringmode thecalculationpivots theinfovectortothex-hubwhilerecording theedge of revolutionis required. The estimationof ai likewisechangesasindicatedby thedesign. Contingentuponthemethodofoperationzandy are thedirecting variables inturnandvectoringmode individually.The lengthofthe vectorincrementsif requiredsmallscalerevolutionsare notimmaculate, sotokeepupaconsistentvector length,the acquired resultsmustbescaledby thescalecomponentK and itis given bythe condition.

$$K=\prod_i K_i \quad (6)$$

III. FFT algorithm

The quick Fourierchange (FFT) isa discreteFourier changecalculationwhichdecreasesthequantity of calculationsrequiredforfocusesfromto,wherelog is thebase-2 logarithm.

FFTs were initially talked about by Cooley and Tukey (1965),inspiteofthefactthatGausshad really depictedthebasicfactorizationventureas aheadofscheduleas1805(Bergland1969,Strang

1993). [2,3,4].A discreteFourierchangecanbe processedutilizingaFFTby methodforthe Danielson-Lanczoslemmaifthequantity offocuses isaforceoftwo.Ontheoffchancethatthequantity

offocusesisnota force oftwo,achangecanbe performedonsetsoffocusescomparing totheprime componentsofwhichismarginally debasedinrate. AneffectivegenuineFourierchange calculationora quickHartley change(Bracewell1999)givesa furtherincrementinpaceby aroundanelementof two. Base-4 and base-8quick Fourier changesuse improvedcode,andcanbe 20-30% speedier than base-2quickFourierchanges.Prime factorizationis moderatewhentheelementsare vast,yetdiscrete FourierchangescanbemadequickforN=2,3,4,5,

7,8,11,13,and16utilizing theWinogradchange calculation [5][7].

FastFouriertransformalgorithmsgenerally fallinto two classes:

a) decimation in time

b) decimation in frequency.

TheCooley-TukeyFFTcalculationfirstadjuststhe info componentsinbit-turnedaroundrequest,and afterthatassemblestheyieldchange(deviation in time). [10]

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The N-pointdiscrete Fourier change ischaracterized by TheN-pointdiscreteFouriertransformisdefined by

$$X(k)=\sum_{n=0}^{N-1}x(n)\cdot e^{-j\left(\frac{2\pi}{N}\right)nk}(k=0,1,\ldots,N-1) \quad (7)$$

TheN-point FFTcan bedeterioratedto rehashed miniaturizedscale operations calledbutterfly operations.Atthe pointwhenthe measureofthe butterflyis r,theFFT operation is knownasaradix-r FFT.For FFT equipment acknowledgment,if stand out butterfly structureisactualizedinthechip,this butterfly unitwillexecuteallltheestimations recursively.Inthe eventthatparallelandpipeline handling proceduresareutilized,aNpointradix-r FFTcanbeexecutedbyN/(rlogN)clockcycles.

Thisdemonstratesaradix-4FFTcanbefourtimesquicker than aradix-2 FFT.

Fig. 1 demonstratesthe general structure of the64pointradix-4 FFT.

Forequipmentacknowledgment ofFFT, multi-bank memory and"setup"tendingtoprocedureare frequently usedto accelerate the memory access timeandminimizetheequipmentutilization. For radix-rFFT,rbanksofmemory are expectedtostore information,andeverymemory bankcouldbetwo-port memory. With "set up" methodology, the r yieldsofthebutterfly canbecomposedbackto the samememory areasoftherinputs,andsupplantthe oldinformation.For thissituation,toacknowledge parallelandpipelinedFFTpreparing,a productive tendingtoplanisexpectedtostay away fromthe information strife. [5][7].

Amainstreamtendingtoconspireforradix-r(r>2) was displayedby Johnson, however due to the modulo-rexpansion,thisstrategyismoderateand the velocityrelies on upon the length ofFFT. Comparing tothe prime components of which is marginally corrupted in velocity. An effective genuine Fourier change calculation or a quick Hartleychange (Brace well 1999) gives a further increment in pacebyaround avariable of two.

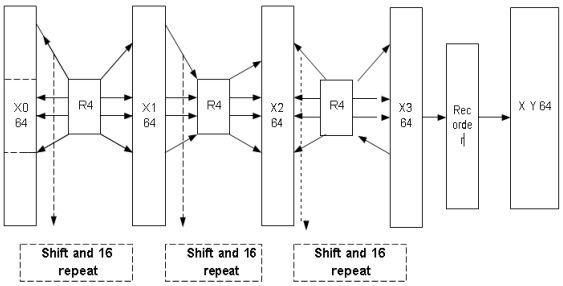

Figure1 RADIX-464pointsFFT architecture

Base-4andbase-8quick Fourier changesuse streamlinedcode,andcanbe 20-30% quicker than base-2 quickFourier changes.primefactorization is moderate when the elements are substantial, howeverdiscrete Fourierchangescanbe made quick forN=2,3,4,5,7,8,11,13,and16utilizing the Winogradchangecalculation

IV. PROPOSEDDESIGN

Inthispaper,lowpowerstrategiesare utilizedfor forceutilizationutilizing reconfigurablecomplex multiplier.UtilizingRadix-2^5calculation,build the computationalpace,further lessenthechipterritory bythreedistinctive handlingcomponents(PE's) were proposed inthis radix-2^5 64-pointFFT/IFFT processor.The proposeddesignutilizesCORDIC calculationtoactualizebutterfly unitstoproduce twiddle variableedge valuesandtodiminishthe truncationmistake. Amideveryemphasisofthe CORDIC calculation, theinfo pointiscontrasted and the steady.

Theproposeddesigncomprisesofabutterfly units, complexBoothmultipliers, complexconsistent multipliers,first-infirst-out(FIFO),controlunitandmultidatascaling squares. The butterfly units performcomplexexpansion and subtraction oftwo informationx[n]what'smore,x[n+N/2].Every info signals in the butterflyunits originatefrom past stage andtheFIFO,separately.Thebutterfly unit1(BU1) behaviors to justcomplexexpansion and subtraction. Inany case,thebutterflyunit2(BU2)incorporates twiddlevariable W4 increaseusinganymultiplexers. The twiddle componentduplicationforFFT calculationisdirectedby settledwidthcomplex multipliers.

The mindboggling increase needs a turn upward table (LUT)utilizing read-justmemory (ROM)to

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store the twiddle componentvalues.Tolessenthe basicway defer,thepipelinedcomplexBooth multiplier was utilized as a part of this FFT processor.Moreover,the mistake remuneration procedurefor thesettledwidthduplicationwas connectedto decreasequantization blunder.The twiddlevariableaugmentationisledutilizing altered widthcomplexmultipliers. Thetwiddle variable qualitiesputaway intheread-justmemory(ROM) are utilizedasthemultiplicandasapartofthe intricateBoothmultiplier. ThealteredBooth calculation isutilized broadly for fast increases. Since themostextremeclockrateof theFFT processorreliesonuponthebasicway ofthe unpredictableBoothmultiplier, three levelpipelined complexBoothmultiplierisutilizedfor rapid operation. Since quantization blunders influencethe sign to-clamor proportion (SNR) execution ofthe framework,amistakeremunerationtechnique[9]is

utilized to lessen thequantization blunder. The proposed FFT processor utilizes consistent multipliers inlightofthe acceptedmarkeddigit (CSD)representationfortheperplexing duplication math in stages 2, 3,and 7.

The twiddle variable W8 has one and only coefficient,yettwiddle components W16andW32 have threeandsevencoefficients,separately.Forthe most part the current examination is utilizing complex Boothmultipliers for the twiddle component W32increase.Be thatasitmay,inour outline,thecomplexCSDsteady multiplierhasbeen utilizedfor thetwiddlecomponentW32 augmentation.

Additionally, the normalsub-expressions sharing (CSS) methodlessensthe equipmentunpredictability ofthecomplexCSDconstantmultipliers[10]. The proposed FFTprocessorappliedCSD constant multiplier insteadofcomplexBoothmultiplier at several stages.

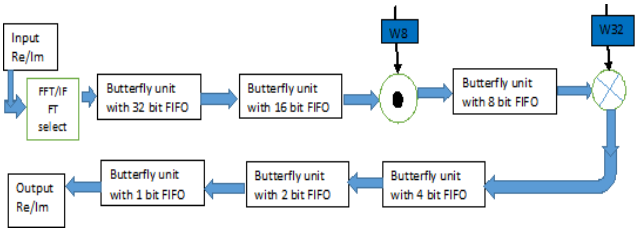

Figure.2aProposedarchitectureof64bitFFT

Theradix2^5algorithmhassamebutterfly structure asradix2,only thechangeistwiddlefactoris available oreachstage.The radix2^5algorithm can be expressed as follows.

n= (N/2n1+N/4n2+N/8n3+N/16n4+N/32n5+n6)N

n1,n2,n3,n4,n5= 0, 1 n6=0…N/32-1

k=(k1+2k2+4k3+8k4+16k5+32k6)N

X(k1+2k2+4k3+8k4+16k5+32k6)

$$=\sum_{n_6=0}^{\frac{N}{32}-1}\sum_{n_5=0}^{1}\sum_{n_4=0}^{1}\sum_{n_3=0}^{1}\sum_{n_2=0}^{1}\sum_{n_1=0}^{1}\times x\left(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+\frac{N}{16}n_4+\frac{N}{32}n_5+n_6\right)W_N^{nk}$$

Thetwiddalfactorcanbeexpressedasfollows:

$$W_N^{\left(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+\frac{N}{16}n_4+\frac{N}{32}n_5+n_6\right)\left(k_1+2k_2+4k_3+8k_4+16k_5+32k_6\right)}$$

$$=\underbrace{(-1)^{n_1k_1}}_{Stage1BU}\overbrace{(-j)^{n_2k_1}}^{Stage1TF}\underbrace{(-1)^{n_2k_2}}_{Stage2BU}\overbrace{W_8^{n_2(k_1+2k_2)}}^{Stage2TF}$$

$$\times\underbrace{(-1)^{n_3k_3}}_{Stage3BU}\overbrace{W_{16}^{(2n_4+n_5)(k_1+2k_2+4k_3)}}^{Stage3TF}\underbrace{(-1)^{n_4k_4}}_{Stage4BU}\overbrace{(-j)^{n_5k_4}}^{Stage4TF}$$

$$\times\underbrace{(-1)^{n_5k_5}}_{Stage5BU}\overbrace{W_N^{n_6(k_1+2k_2+4k_3+8k_4+16k_5)}}^{Stage5TF}W_{\frac{N}{32}}^{n_6k_6}$$

(8)

Proposed architectureisshowninfigure.2a.Figure 2bshowsthe signalflow graph of 64 bitFFT.Also twiddle factorgenerationimplemented using CORDIC algorithm as shown in figure3.

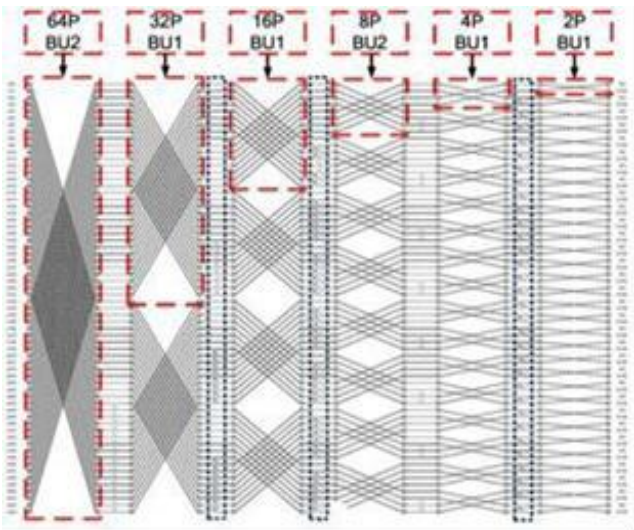

Figure2b.Signalflowgraph64pointFFT

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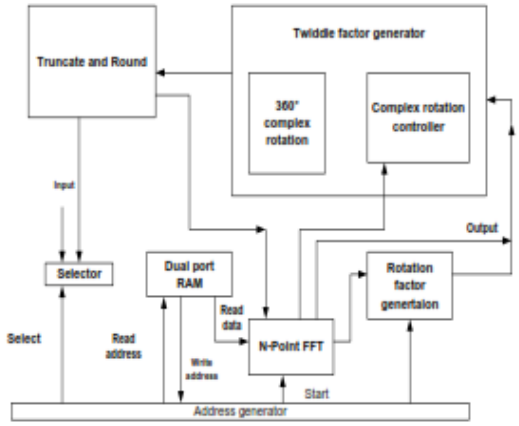
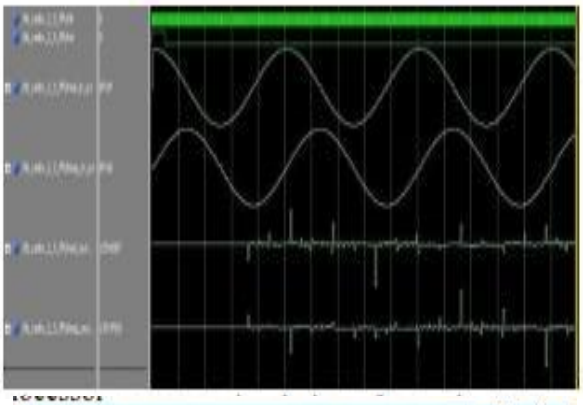
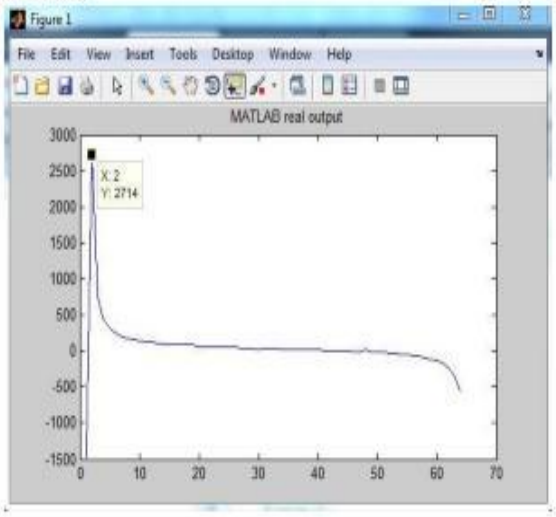


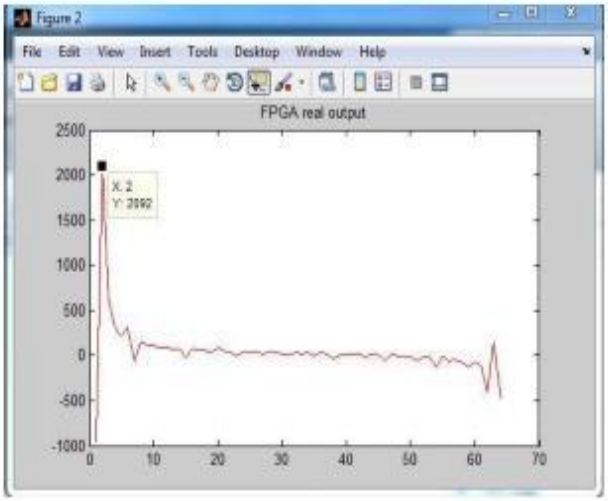
Figure3.CORDICalgorithmstructureforbutterfly unit

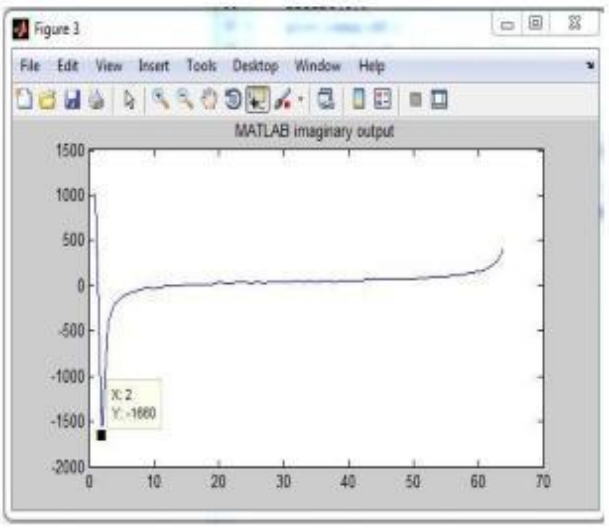
V. VHDL andMATLAB simulationResults

64pointFFTRealandimaginary outputsare shown infigureswhicharecompareusing matlaband FPGA.Alsocomparedwithother designsofFFTas shown in table 1.









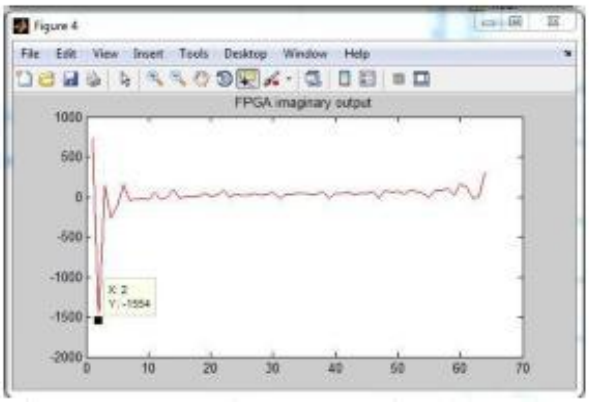


Figure4.Realandimaginaryoutputsfor64 pointFFT

Implementation	No. of 4 LUTs used	No. of occupied slices used	No. of Bonded IOBs used	No. of BUFG-MUXs used	Maximum frequency (MHz)
Reference[9]	487	----------	36	12	----
Reference[10]	1202	147	7	1	140.308
Proposed design mixed radix FFT/IFFT	207360	122	45	1	420.203

Table 1 ComparisionTable

VI. CONCLUSIONS

InthispaperRadix-2^5FFTprocessorarchitectureisstudied.Forgeneration of twiddlefactorCORDIC algorithm isused.Various parts ofFFT architecture suchasButterfly unit,ControlUnit,Delay-Feedback modelare discussed.Proposedresearchwork emphasesonthe use of techniques toreducethe computationalcomplexityofprocessordesignand the algorithmused which resultinto improvement of thedesign significantlyforvarious OFDM based applicationforlowpowerconsumption.

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