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Design and Implementation of an Efficient Content Addressable Memory Using Early-Predict Scheme

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ABSTRACT

Content-addressable memory (CAM) is a special type of memory which can do search operation in a single clock cycle and it is a hardware for parallel lookup/search. The parallel search scheme promises a high-speed search operation but at the cost of high power consumption. This paper presents a novel Early-Predict Scheme to design a high performance Content Addressable Memory with lower power consumption and high speed as compare to other existing CAMs. First technique is NOR-type and NAND-type Precharge techniques CAMs are suitable for high-search-speed and low-power consumption application respectively. Second technique is Precharge-Free technique CAMsare suitable for low-power consumption application. The Early-Predict Scheme CAMs are suitable for both high-search-speed and low-power consumption application. The experimental results show that upto 74.40% power savings can be obtained and 52.56% Speed increased as compared to conventional CAM design.

Index Terms—Content-addressable memory(CAM), high-speed search, low power, NAND-type Precharge, NOR-typePrecharge,Prechargefree,Early-predict.

1. INTRODUCTION

Content Addressable Memory (CAM) compares the inputsearch data against a stored data and returns the address ofmatched data. Due to parallel operation the throughput isobtained in one clock cycle which makes it faster [5].However CAM can consume more power, because thematched line on the CAM's output consists of large parasiticalcapacitance, due to which large charge power is beenconsumed [18]. It has wide applications like Computernetwork device, data compression, database management anddisk caching, pattern and image recognization. The parallelsearch scheme of the CAM activates a large number of circuitsduring the search operation and therefore needs more power[1],[6].Designing a low power CAM for a large number of bits of aword without degrading its function (high-speed search) is achallenging task.

2.CONTENT-ADDRESSABLE MEMORY

CAM contains memory elements, usually built with 6T SRAM cell and the circuit is compare searchbit with the store bit.

3.NOR-type and NAND-type Precharge Technique CAMs

NOR-type and NAND-type Precharge Technique CAMs [23] are widely used in most of thedesigns. Fig.1 (a) and (b) shows the NOR-type and NAND-type Precharge technique CAMs respectively. In these CAMs the matchline MLs are precharged.For every precharge cycle, the ML will be precharged. If all the bits in a word match with the search bits then ML will hold its precharged valueIn the case of mismatch of the bit or bits, a pull-down path through the mismatched CAM cell is formed for the ML to drain its precharged value.

CAM has many existing methods in that NOR- type precharge technique have high search speed but it have high power consumption and NAND- type precharge technique have low power consumption but its performance is very low as compared to NOR match line. So the disadvantage of NOR type CAM is high power consumption and disadvantage of NAND type CAM is search data speed is high.

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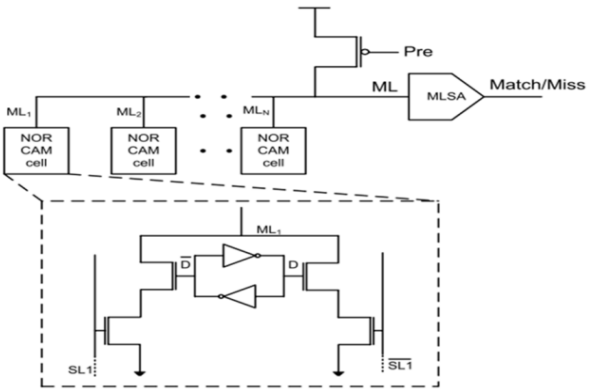

Fig.1. (a)NOR-type Precharge CAM.

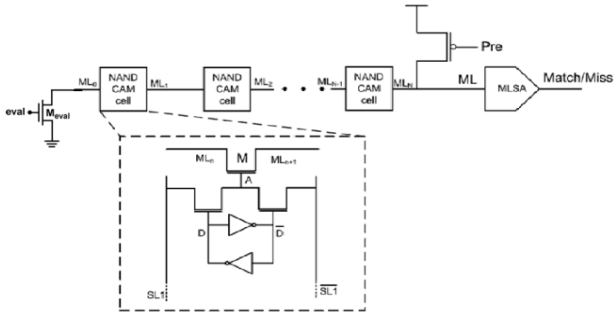

Fig.1. (b) NAND-type Precharge CAM.

4.CAM WITH PRECHARGE-FREE TECHNIQUE

The gate of one NMOS transistoris connected to search bit SL, and its source is connected to stored bit D of its SRAM cell. Another gate of one NMOS transistor is connected to complementary of search bit SL, and its source is connected with complementary stored bit D of its SRAM cell. CAM architecture i.e. free from all disadvantages of above, which are present in the existing CAMs. In the Precharge-free CAM, as shown in Fig. 2, 8T CAM cells formthe basic building block. This is similar to the NAND-typeML, except that the pass transistor is excluded. If the searchbit matches with the stored bit, then ML will get charge eitherfrom D or $\overline{D}$; else ML will be isolated from both D and $\overline{D}$.

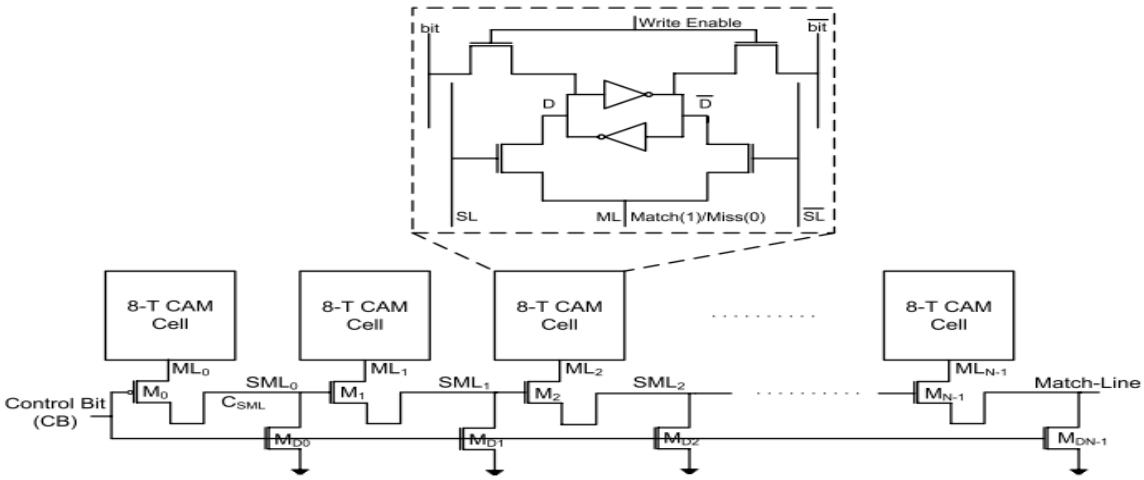

Fig.2.CAM with Precharge-Free technique.

4.1.OPERATION

If the control bit (CB) is set to logic zero and all the pull-down transistors in cut off region, the CB and the pull-down MOS transistors M_{D0}–M_{DN-1} together serve the purpose of resetting the ML segments between two successive searches. If the first bit of a word in the CAM matches the first search bit, M_{L0} goes high and it drives M_0 into saturation region to charge SML_0.WhenSML_0 charges, M_1turns into saturation region. Similarly, if the second bit also matches, then SML_1 charges and M_2 attains saturation. If all the bits in the stored word match with the bits in the search word, then the Match-Line becomes high. In this case let us say, the second bitmismatches with the stored bit, then SML_1 will not charge and M_2 remains in the cut off region. Thus SML_1 doesn'tprecharge and M2 remains in cut off region. Due to this, the Match-Line is discharged to 0 [23].

5. CAM WITH EARLY PREDICT TECHNIQUE

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Two pairs of nMOS are connected in series with the SRAM cell such that the gates of one pair of nMOS are connected to the stored bit (D) and thecomplement of search bit ($\overline{SL}$)andthe gates of anotherpair of nMOS are connected to the complement of stored bit ($\overline{D}$)and search bit (SL).In the novel CAM, as shown in Fig. 3, 6T CAM cells formthe basic building block.This is similar to the NOR-type Precharge CAM, except that the Precharge controller is excluded.

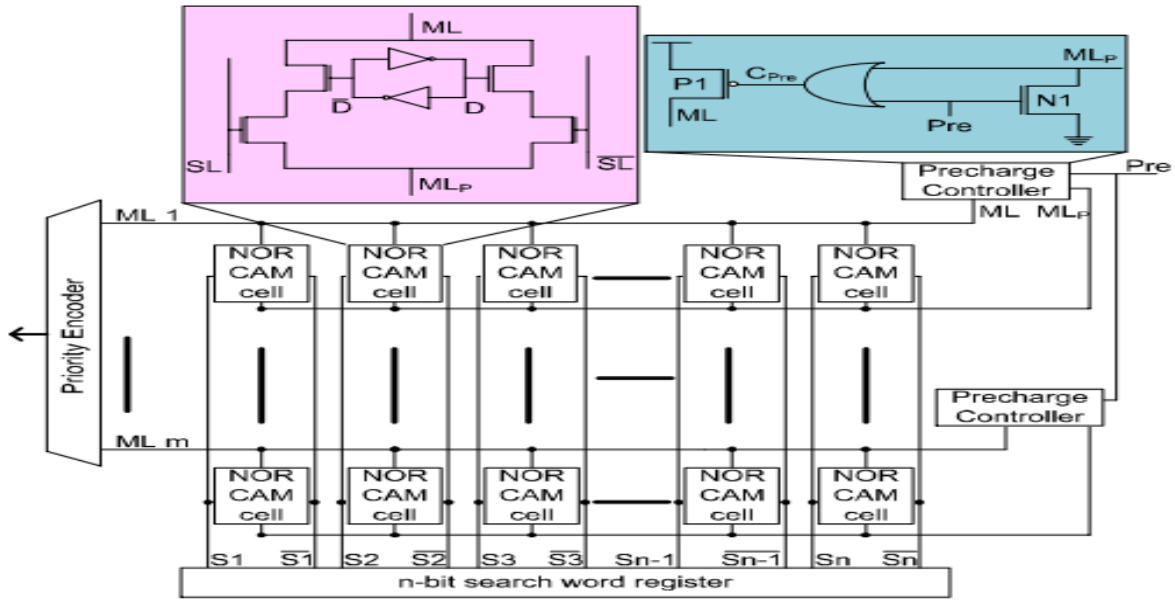

Fig.3. CAM with Early-Predict Scheme.

5.1.**OPERATION**

In novel CAM, content addressable memory precharges all the MLs (ML_1 to ML_m).When Pre signal is low and evaluates match/miss of the search data.When Pre goes highfor every precharge cycle, the ML will be precharged, If all the bits in a word match with the search bits then ML will hold its precharged value.In the case of mismatch of the bit or bits, a pull-down path through the mismatched CAM cell is formed for the MLs drain their charge denote zero.This reduces the voltage swing of the mismatching MLsto improve the CAM performance. It is unnecessary to charge themismatching MLs to full swing level, since those MLs had been discharged in the evaluation phase. Unlike conventional CAMarchitectures, which during the precharge phase simply charge the MLs, the novel CAM also predicts the MLs that would mismatchearly in the precharge phase.

All MLs are precharged through a precharge controller as showed in fig.3. The Early-Predict CAM design dynamically varies the precharge time,so as to stop precharging of the mismatching MLs to full level. Pre is a fixed precharge signal and CPre is a dynamicallyvarying precharge signal. If the search data mismatches with the word connected to ML, a path between the nodes ML and ML_P is created.When the MLs start to precharge, node ML_P gets charge throughthe mismatching XOR circuit of the CAM cell from the node ML.As node ML_P reaches to threshold value which is connected in parallel tonMOS in the OR gate, CPre starts rising to halt ML from gettingfurther charge.

6.SIMULATION RESULTS

The CAM with Precharge-free technique and Early –Predict scheme CAM design are implemented using Tanner tool 16.0 version software tool, 0.13µm CMOS technology is used. The power consumption and speed of operation of the NOR-type Precharge, NAND-type Precharge CAMs, Prechagre-Free CAM and Early Predict scheme CAM designs are compared.

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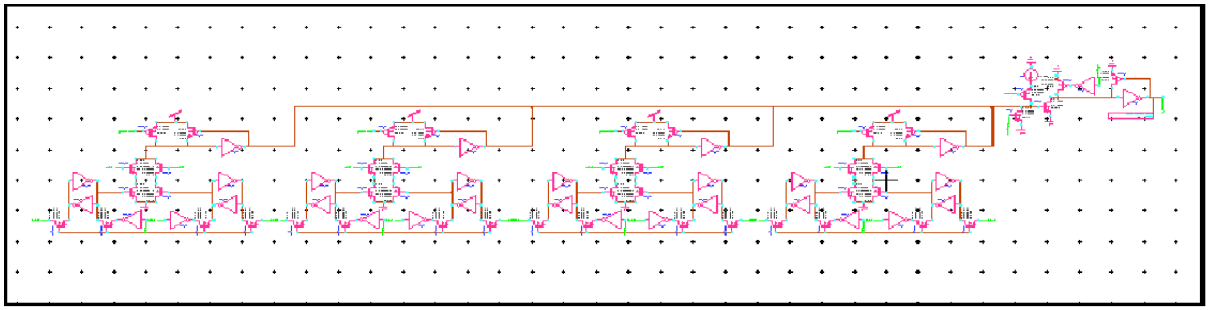

Fig 4.1(a) Circuit schematic of Conventional CAM with comparison and storage parts.

Figure 4.1(a) shows the Schematic of 4-bit Conventional CAM. Here four CAM cells are connected in series. Each CAM cell has comparison logic and storage parts.

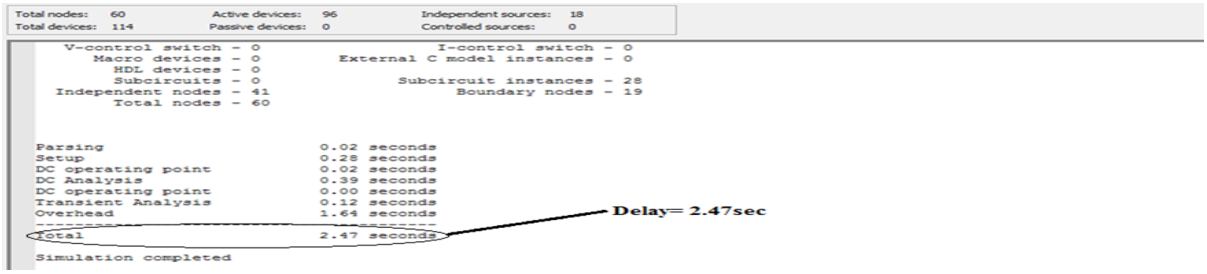

Fig 4.1(b) Speed analysis of Conventional CAM.

Figure 4.1(b) shows theConventional CAM,Speed analysis. The speed obtained is 2.47 Seconds.

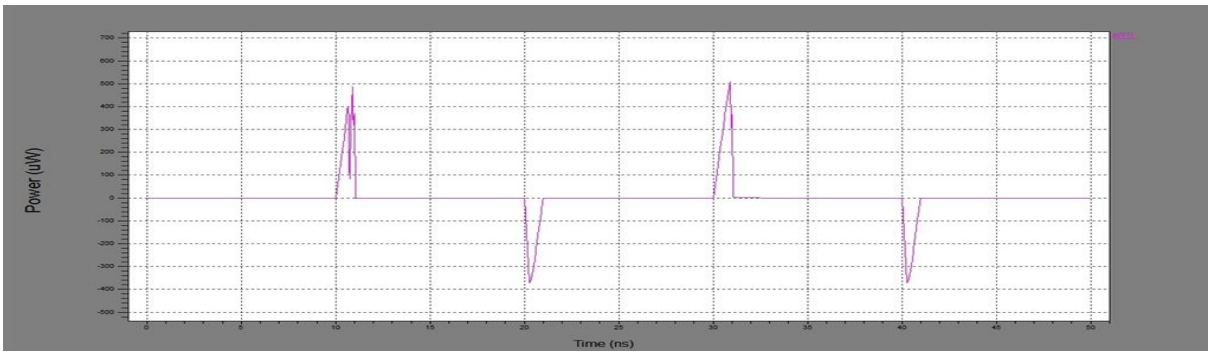

Fig 4.1(c) Power analysis of Conventional CAM.

The figure 4.1(c) shows the power analysis of conventional CAM. The powerconsumption obtained is 508µW.

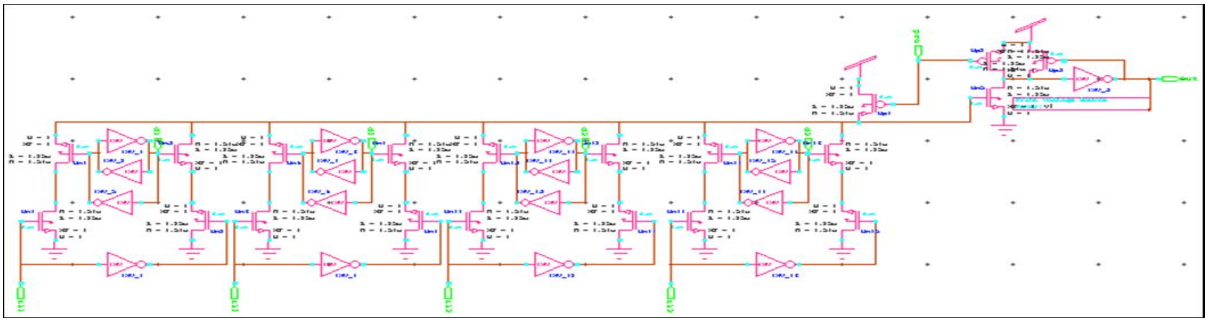

Fig 4.2(a) Circuit schematic of NOR-type Precharge CAM with comparison and storage parts.

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Figure 4.2(a) shows the Schematic of 4-bit NOR-type Prechargetechnique CAM. Here four CAM cells are connected in series. Each CAM cell has comparison logic and storage parts.

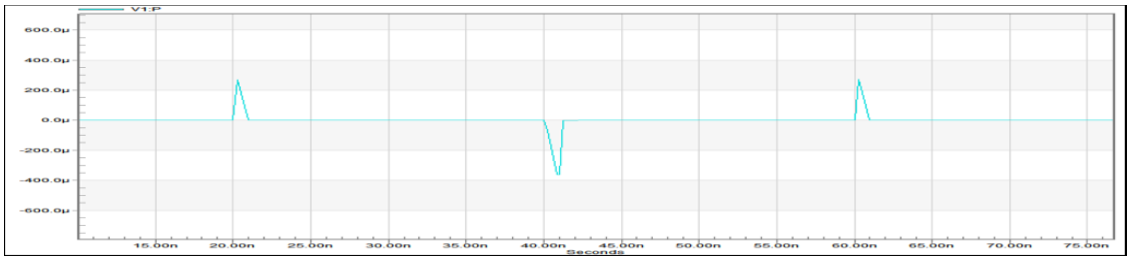

Fig 4.2(b) Power analysis of NOR-type Precharge CAM.

The figure 4.2(b) shows the power analysis of NOR-type Precharge CAM, which is used to compare thepower reduced value to that of various implemented power reduction techniques. Here the powerconsumption obtained is 271µW.

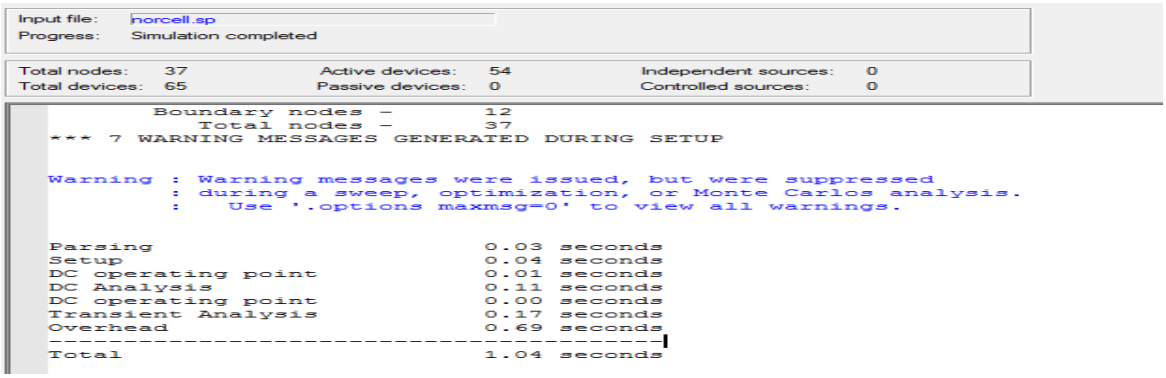

Fig 4.2(c) Speed analysis of NOR-type Precharge CAM.

Figure 4.2(c) shows theSpeed analysisof NOR-type Precharge CAM. The speed obtained is 1.04 Seconds.

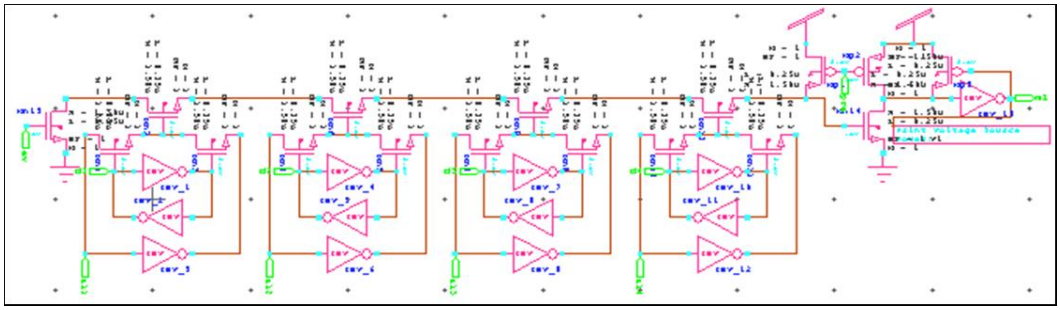

Fig 4.3(a) Circuit schematic of NAND-type Precharge CAM with comparison and storage parts.

Figure 4.3(a) shows the Schematic of 4-bit NAND-type Prechargetechnique CAM. Here four CAM cells are connected in series. Each CAM cell has comparison logic and storage parts.

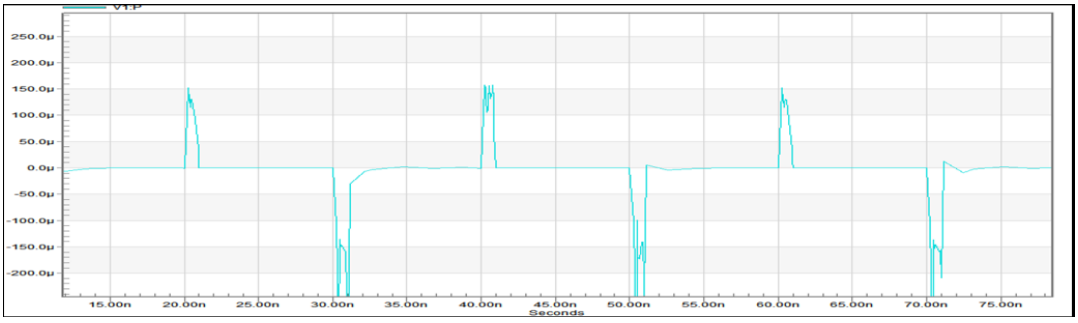

Fig 4.3(b) Power analysis of NAND-type Precharge CAM.

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The figure 4.3(b) shows the power analysis of NAND-type Precharge CAM, which is used to compare thepower reduced value to that of various implemented power reduction techniques. Here the powerconsumption obtained is l44µW.

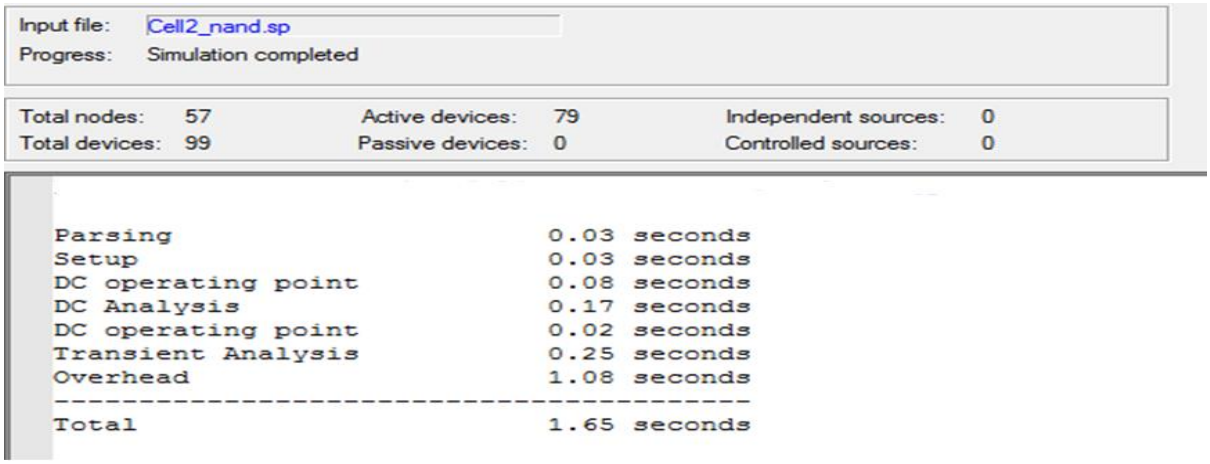

Fig 4.3(c) Speed analysis of NAND-type Precharge CAM.

Figure 4.3(c) shows the NAND-type Precharge CAM,Speed analysis. The speed obtained is 1.65 Seconds.

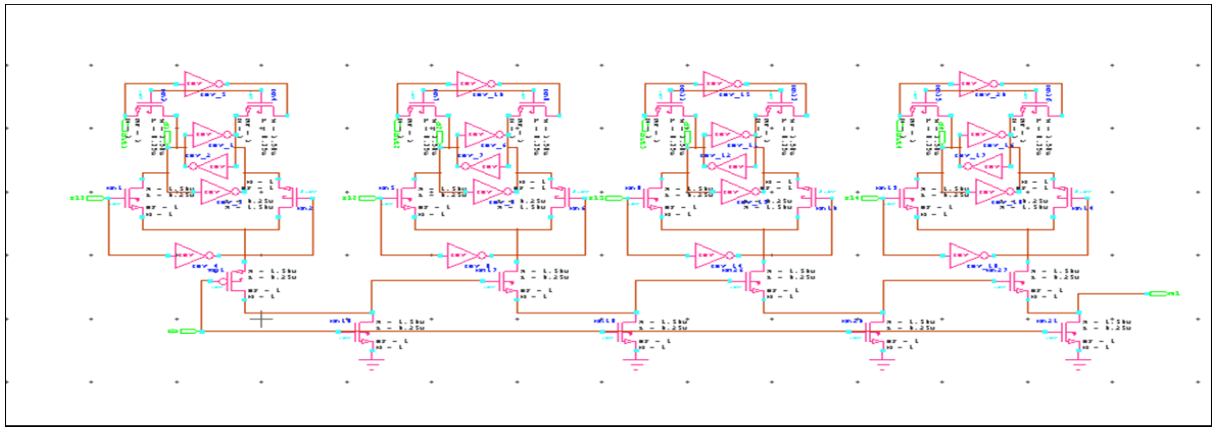

Fig 4.4(a) Circuit schematic of Precharge-free CAM with comparison and storage parts.

Figure 4.4(a) shows the Schematic of 4-bit CAM with Precharge-Free technique. Here four CAM cells are connected in series. Each CAM cell has comparison logic and storage parts.

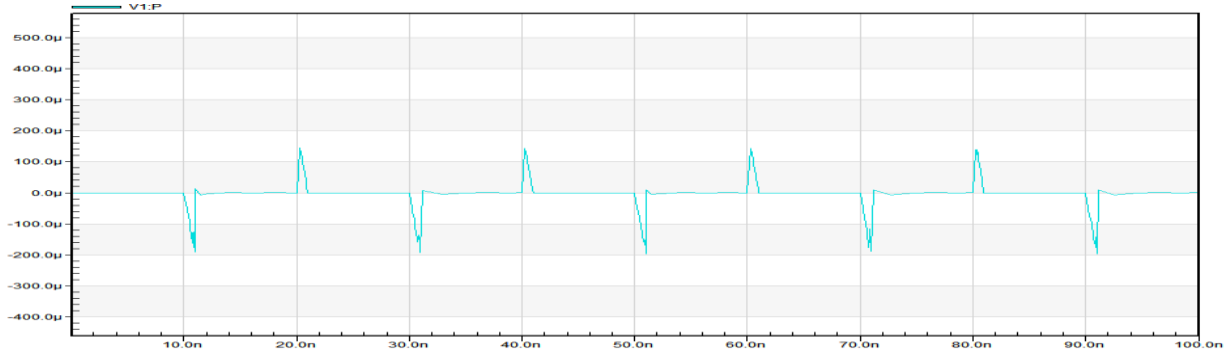

Fig 4.4(b) Power analysis of Precharge-free CAM.

The figure 4.4(b) shows the power analysis of Precharge-Free CAM, which is used to compare thepower reduced value to that of various implemented power reduction techniques. Here the powerconsumption obtained is l44µW.

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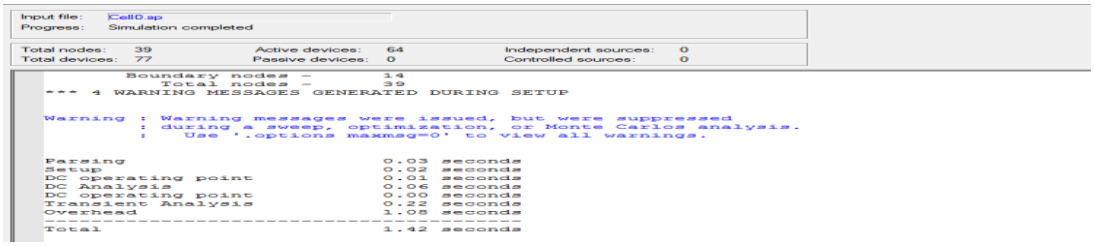

Fig 4.4(c) Speed analysis of Precharge-free CAM.

Figure 4.4(c) shows the Precharge-Free CAM,Speed analysis. The speed obtained is 1.42 Seconds.

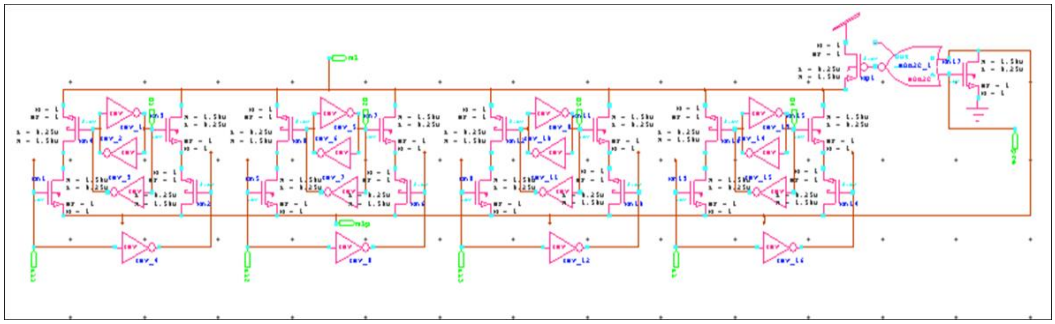

Fig 4.5(a) Circuit schematic of Early Predict(Novel) CAM with comparison and storage parts.

Figure 4.5(a) shows the Schematic of 4-bit CAM with Early Predict Scheme. Here four CAM cells are connected in series. Each CAM cell has comparison logic and storage parts. Here Precharge controller is control the power.

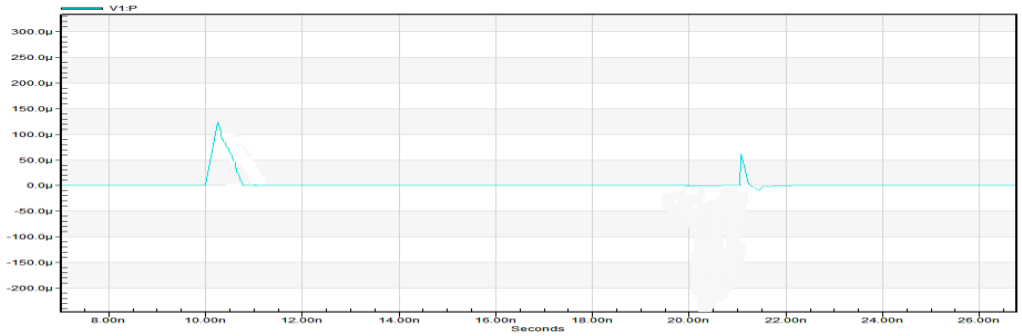

Fig 4.5(b) Power analysis of Early Predict Scheme (Novel) CAM.

The figure 4.4(b) shows the power analysis of Early Predict scheme (Novel) CAM, which is used to compare thepower reduced value to that of various implemented power reduction techniques and Precharge-Free Technique. Here the powerconsumption obtained is l30µW.

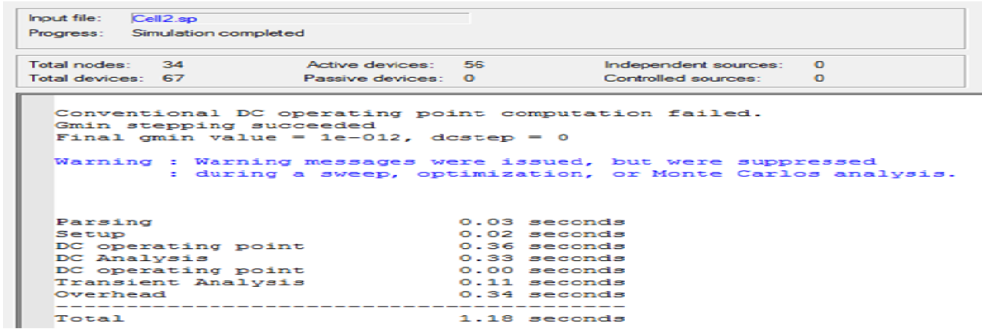

Fig 4.5(c). Speed analysis of Early Predict scheme (Novel) CAM.

Figure 4.5(c) shows the analysis of Early Predict scheme (Novel) CAM. The speed obtained is 1.18 Seconds.

7. TABLE.I

Performance Comparisons of various CAM Techniques

	Power(µ watts)	**Speed(sec)**	**Power reduced compare to CAM**	**Speed increased compare to CAM**
Conventional CAM	508	2.87		
NOR-type Precharge technique CAM	271	1.04	46.65%	57.89%
NAND-type Precharge technique CAM	156	1.65	69.29%	33.19%
Precharge-free technique CAM	144	1.45	71.65%	41.29%
Early Predict scheme (novel) CAM	130	1.18	74.40%	52.26%

8.CONCLUSION

An energy efficient content addressable Memory design is proposed in this paper. The reduction of high power consumption and search delaywhich are the limiting factors of CAMs has been achieved by Early predict scheme which is implemented in 0.18 µm CMOS technology. The Early Predict scheme is designed in which power is reduced up to 74.40% and increased speed up to 52.26% compared to Conventional CAM.

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