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Design & Analysis Of Three Phase Multilevel Inverter With Lower Switching Costs For Solar Application

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Abstract—*In this paper, how the switching cost and total harmonic distortion can be reduced by using new topology of multilevel inverter. These topology can be extended for any level of multilevel inverter. In this paper, the mode of operation for 5-level inverter can be discussed, similarly modes of operation for higher level can be analyzed. This paper also demonstrate the simulations of seven level 3-φ multilevel inverter. This new topology shows that the three single phase multilevel inverter build a three phase seven level multilevel inverter, It also presents the seven inverter along with harmonic reduction and less number of switching components. The harmonic reduction can be achieved by selecting appropriate switching angle. This proposed technology contains advantage to it's less number of components in comparison with cascade H-bridge multilevel inverter. Basically in this inverter, reducing THD and number of switches so that we may get optimum power flow and smooth shine wave shape, thus it is very appropriate to connect with grid.*

Keywords-THD (Total Harmonic Distortion), Multilevel, H-bridge, switching time

I. INTRODUCTION

Multilevel inverter:-An inverter is a power electronics equipment which is able to provide appropriate ac voltage state at the output port using numerous lower DC voltages. The multilevel inverter gives output waveform with lower harmonics and dv/dt. Smoothness of the voltages is proportional to the voltage level but complexity of controller circuit increases with increased stages. For improving wave shape and reducing THD, here four level multilevel inverter is used. The performance of this technic far better than conventional type line commuted inverter. This methodology reduces THD, switching losses, and EMI.As we are aware fossil-fuel supply coal, petroleum, and natural gas will be depleted in few hundred years unless we exploit other sources of energy. Alternative new, non-conventional, renewable and clean sources are to be developed for future energy requirements. The Inverter is used solar application as shown in fig.-1 [2]

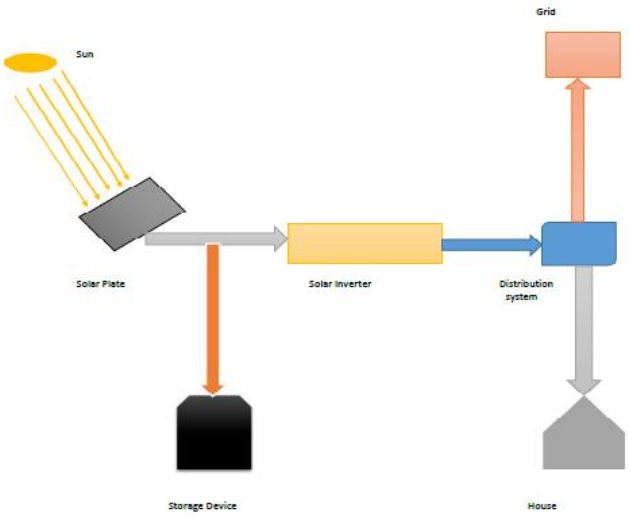

Fig.-1: Application of Solar Inverter

II. CASCADE TYPE H-BRIDGE MULTILEVEL INVERTER

For analysis of multilevel waveform the AC output voltage of different level of H-bridge cell is connected in cascade form, the sum of the total H-bridge cell output gives the out of the inverter. For the cascade form, m=2s+1; Where s is the number of DC sources, m=Voltage level stage In general we have to find total voltage of m-level inverter for single phase $V_{AN}=V_{dc1}+V_{dc2}+\ldots\ldots\ldots+V_{d(s-1)}+V_{ds}$

Where s= No. of DC sources.

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Because zero voltage is common for all H-bridge cascade inverter output thus the total number of voltage level is 2s+1.Now we have assumed $V_{dc1}=V_{dc2=}.....V_{dc(s-1)=}V_{dcs}=V_{dc}$ Single phase configuration of an m-level H-bridge cascade inverter shown in diagram in fig.-2 [1,4&6]

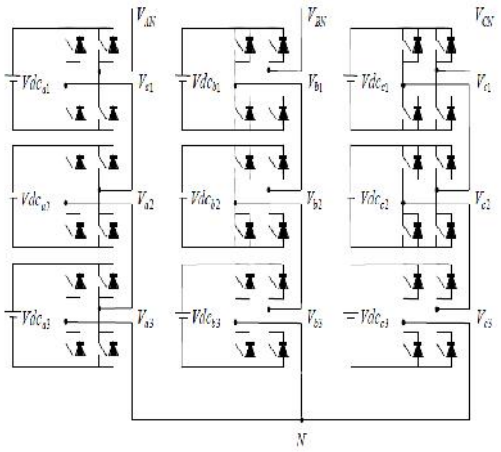

Fig.-2: Three phase seven level multilevel inverter

As we know that line voltage can be represented in terms of two phase voltages. For the example the line voltage between A and B is so called V_{ab}

$V_{ab}= V_{an} – V_{bn,}$ Where V_{ab} = line voltage,

Van= Voltage of phase A w.r.t point N

V_{bn} = Voltage of phase B w.r.t point N

All triplet harmonics component in line voltage can be eliminated in three phase multilevel inverter, however this type of harmonics component can be eliminated by one third cycle phase shift feature.

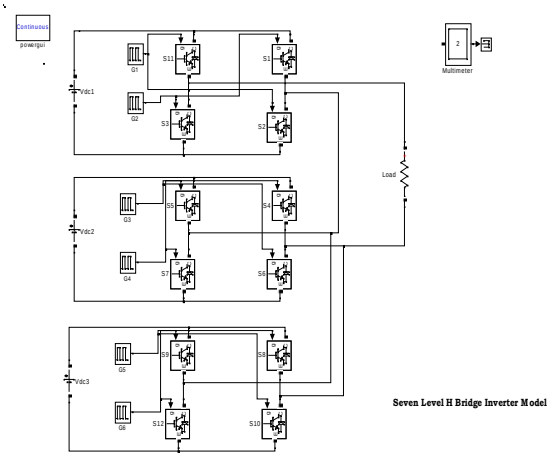

Fig.-3: Schematic of seven level conventional H-bridge 7- level inverter

Seven level conventional H-bridge 7- level inverter is simulated as shown in fig.-3.Here also three voltage sources having equal in magnitude are applying.

III. NEW TOPOLOGY BASED MULTILEVEL INVERTER

This topology demonstrates how to reduce total harmonics distortion can be obtained by new methodology of multilevel inverters. This technology contains advantage to it's less number of components in comparison with cascade H-bridge multilevel inverter, this topology can be extended for any number of level. In this chapter here, we will discuss 1-φ 5-level and 1-φ 7-level multilevel inverter and also compare among these.[4] This report consists modification of 7-level inverter in MATLAB simulation. Basically in this inverter, we are reducing THD and number of switches so that we may get optimum power flow and smooth shine wave shape. Reduction of total harmonic distortion can be achieved by selecting suitable switching angle. Now at first, we will discuss 5-level inverter based new topology as shown in fig.-4.

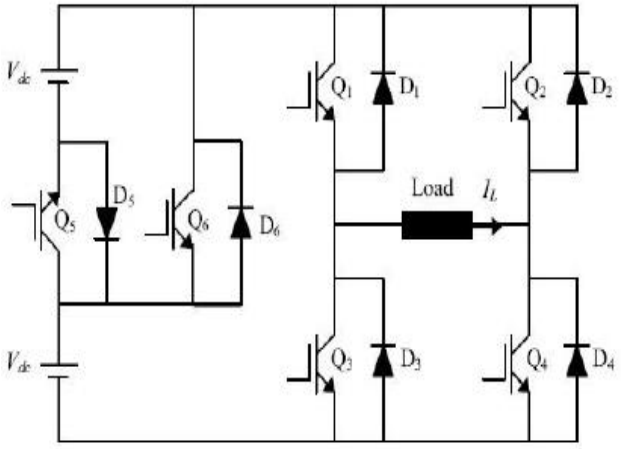

Fig.-4: Five level inverter based new topology

Basically there are three operating mode of this inverter.

- ✓ Powering Mode
- ✓ Freewheeling mode
- ✓ Regenerating mode

Powering mode:

Powering modes are described as shown in table1. [4]

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Table 1: Powering mode of 5-level inverter

Mode Type	Path of the current	Voltage
1	Lower V_{dc} source →D_6→Q_1→Load→Q_4→lower V_{dc} source	**+V_{dc}**
2	Lower V_{dc} →Q_5→ Upper V_{dc}→Q_1→Load→Q_4→Lower V_{dc} source	**+2V_{dc}**
3	Lower V_{dc} source→D_6→Q_2→Load→Q_3→Lower V_{dc} source	**-V_{dc}**
4	Lower V_{dc} source→Q_5→Upper V_{dc} →Q_2→load→Q_3→Lower V_{dc}source	**-2V_{dc}**

Freewheeling mode:

Freewheeling mode are active, if one of the main switches are turn off while load current needs to continue it's pass. This mode can be achieved by the help of antiparallel diodes of the main switch. In this mode the positive half cycle current pass through Q_1, load, D_2 or Q_4, Q_3, load. For negative half cycle the current be continued through Q_3, load, D_4 or Q_2, load, D1 as shown in fig. 4 [4]

Regenerative mode:

In this mode, part of the energy stored in load inductance is back to the source it happens when the load current is negative during the positive half cycle and vice versa. In this interval output voltage is zero, when the positive current passes load, D2, Q6, the lower V_{dc}, D_3. For negative current passes load D_1, Q_6, lower V_{dc}, D4. [4]

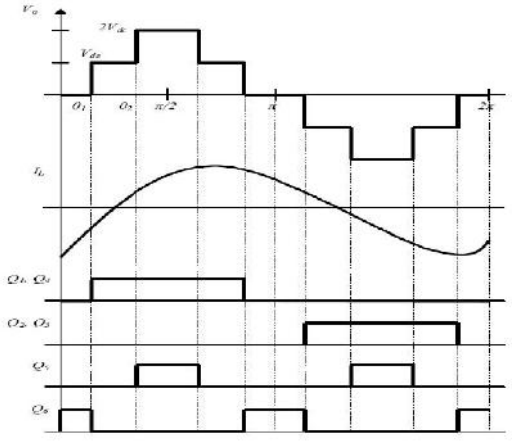

Fig.-5: Wave form of five level inverter based new topology.

Now we can generalize in circuit configuration of the new topology is shown in fig.6 this advised topology gives the advantages of less number of switches. But it has also a draw backs, due to using of less number of switches, the rating of load switches has to be increased, these high rating switches having high cost.[3&4]

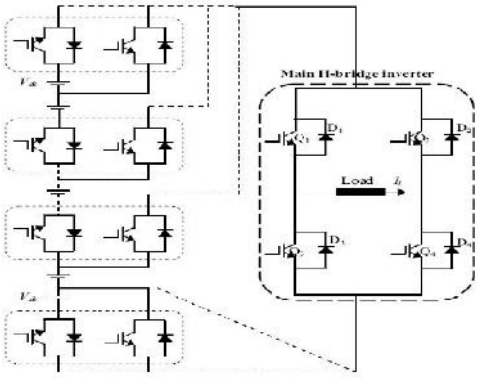

Fig.-6: New topology based generalized configuration of multilevel inverter.

IV.DESIGN AND ANALYSIS OF 7-LEVEL 3-Φ MULTILEVEL INVERTER WITH LOWER SWITCHING COSTS FOR SOLAR APPLICATION

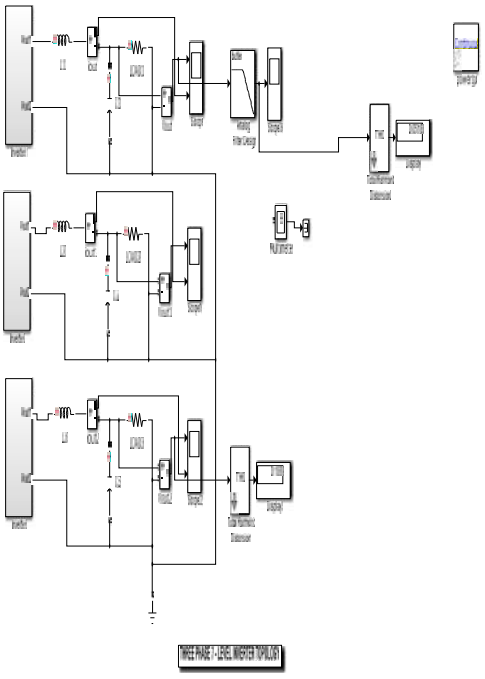

Fig.-7: Deign of 3-φ seven level multilevel inverter with less number of switches.

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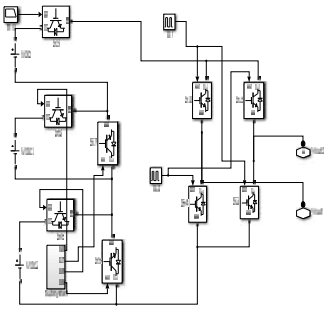

Fig.-8: Design of 1-φ seven level multilevel inverter

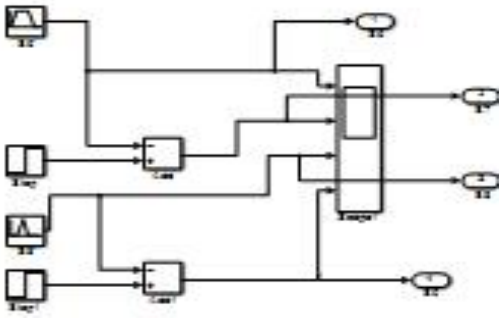

Fig.-9 Simulation of subsystem for providing gate signal

In this proposed topology we simulate 1-φ 7-level multilevel inverter the multilevel inverter contains 9 number of switches(S_1,S_2,S_3,S_4,S5,S_6,S_7,S_8,S_9), 3 number of DC sources(V_{dc},$V_{dc1}$and V_{dc2})and 1 inductor as shown in fig.30. Here we have modified with less number of switches, lower switching loss, lower switching cost, optimum power flow and reduced total harmonic distortion.

Each smaller multilevel unit will produce a voltage of V_{dc} therefore V_o (Output voltage) will be equal to $3V_{dc}$ as shown in table 2. H-bridge is added to the circuit for creating both positive and negative voltage level.3 levels will appear in positive half and 3-levels in negative half cycle and including zero level, therefor, the total seven levels can be created. The total switch count is 9 for a seven level inverter were as for a conventional cascade multilevel inverter, it is 12.

In this proposed topology applying three voltage source V_{dc}, V_{dc1} and V_{dc2} having magnitude 90V.

The nine switches are operated on the basis of switching logic (ON&OFF) as shown in table: 2

Table: 2 Switching states of proposed topology

State	Switching Positions									Output voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	
1	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	V_{dc}
2	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	$V_{dc}+V_{dc1}$
3	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	$V_{dc}+V_{dc1}+V_{dc2}$
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
5	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	$-V_{dc}$
6	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	$-V_{dc}-V_{dc1}$
7	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	$-V_{dc}-V_{dc1}-V_{dc2}$

V. SIMULATION RESULTS

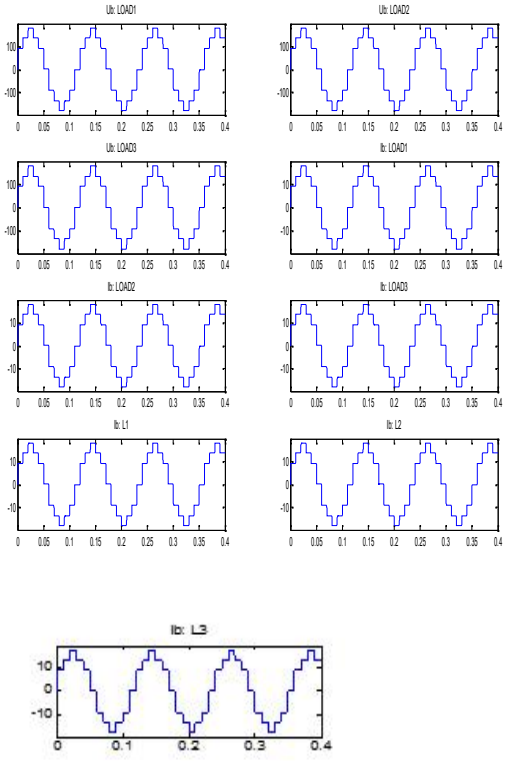

Fig.-10: Wave form Output voltage across Load, output current across load, Current of inductor L_1 and voltage of capacitor C.

The proposed topology has the advantage of its reduced number and THD % value is 5.185 which is lowest as IEEE standard.[8]

Fig.-11: Output voltage of Inverter as seen in the scope

Table 3: Reduction of switching devices in percentage.

S.No	Inverter Type	Number Of switches	% Of Reduction in Switches
1	3-φCascade Type7-level	36	25
2	Proposed 7-level	27	

Table 4: THD value data and reduced percentage

S.No.	Inverter Type	THD Value	% Of Reduction in THD
1.	Cascade Type 7-level Inverter	28.37	81.72
2.	Proposed 7-level Inverter	5.185	

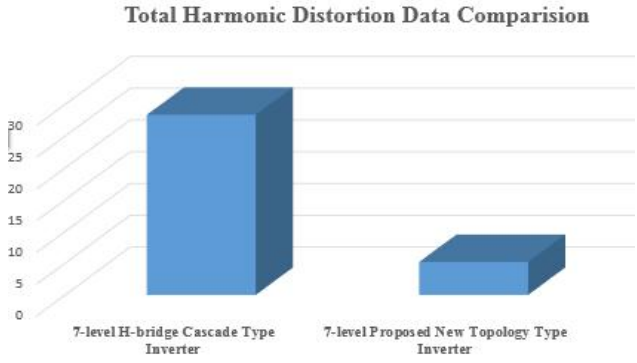

Fig.-12: THD Data Comparison between Cascade type and proposed topology

6. CONCLUSION

A latest family of multilevel inverter has been simulated in MATLAB-Simulink. In this paper we simulate 3-φ seven level by using three identical 1-φ seven level multilevel inverter. It present many advantages its less number of switching device compared to conventional type similar multilevel inverter. However as we increase load, then rating of four main switches should be increased, thus this type of inverter is only applicable for medium voltage range. The operation of switches are based on new topology. A SPWM is applied to the four main switches while switching logic is provided for other five switches which is shown in table no.2. Applying of pulse depends on the resultant of solution of polynomial equation, where the solution gives lowest THD approximate 5% which specifies to IEEE standard. This simulation result prove that this algorithm of proposed topology can be more suitable for elimination in higher order of harmonic and it will give result lowest THD voltage at output of the inverter.

REFERENCES

[1] Dr. Keith Corzine, University of Missouri Rolla "***Operation and Design of Multilevel Inverter***" developed for the office of Naval Research December-2003, Revised June-2005

[2] Riad Kadri, Jean-Paul Gaubert, *Member, IEEE*, and Gerard Champions, *Member, IEEE," **An Improved Maximum Power Point Tracking for Photovoltaic Grid-Connected Inverter Based on Voltage-Oriented Control**"* IEEE transactions on industrial electronics, vol. 58, no. 1, January 2011

[3] N Khader Basha, M Abid Nayeemuddin***" A New Cascaded Multilevel Inverter with less no of Switches***" IJRET: International Journal of Research in Engineering and Technology, Sep-2003

[4]K.Surya Suresh and M.Vishnu Prasad "***Analysis simulation of new seven level inverter"*** International Journal of Scientific and Research Publications, Volume 2, Issue 4, April 2012

[5]Agam Kumar Tyagi, MATLAB and Simulink for Engineers, Oxford university press, Third impression 2013

[6] *Adil Sarwar &M. S. Jamil Asghar, "**Multilevel Converter Topology for Solar PV Based Grid-Tie Inverters**"* 2010 IEEE International Energy Conference

[7] Rajesh Singh Farswan and B. G. Fernandes," ***A New Type of "Buck in Buck, Boost in Boost" Grid-Tied Inverter***" IEEE International Energy Conference2014

[8] Pushkar Kumar, "***Optimal power Flow&THD Reduction using multilevel technique Based Grid Tie-Inverter For PV Application"*** International Journal of Electronics, Electrical and Computational System(**IJEECS),** ISSN 2348-117X ,Volume 6, Issue 6 June 2017