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Performance Analysis of Different Dynamic CMOS Logics

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ABSTRACT

The choice of the CMOS logic to be used for implementation of a given specification is usually dependent on the optimization and the performance constraints that the finished chip is required to meet. Dynamic logic performance is better for higher fan in and complex logic circuits and also with the increasing level of integration, high speed and low power dissipation have become the mandatory requirements for any logic design along with the performance.

Many design logics are available within Dynamic Logic stream. One of the popular logic is the Domino logic for low power dissipation and high speed.

This paper presents a comparative study and analysis of dynamic logic and types of Domino Logic.

KEY WORDS: Domino CMOS circuits, Dynamic Logic, Precharge, Evaluation,Pseudo buffer, Power consumption, Logic synthesis

1. INTRODUCTION

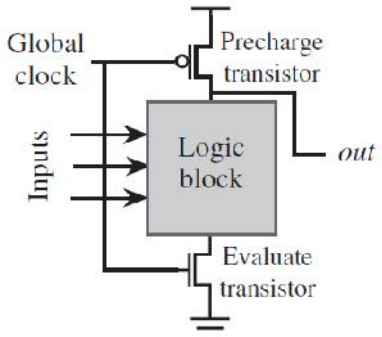
Dynamic logic consumes less power and provides high speed than static logic (**R.L.Geiger** et al 2013). Manufacturing industries continues to give more attention on low power and high speed logic design circuits . Dynamic logic offers a solution to this. Though Dynamic logic provides many advantages, the logic suffers from cascading problem, i.e. when cascading one gate to the next (P**. Gronowski** et al 2001). The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error(**Knepp**er et al 2002).

Thus to cascade dynamic logic gates, one solution is Domino Logic, which inserts an ordinary static inverter between stages. While using domino logic we are using a pFET (Since one of the objective of using Dynamic Logic is to avoid pFETs where possible, due to their low speed), the two reasons it works well are, First, there is no fan out to multiple pFETs.

The dynamic gate connects to exactly one inverter, so the gate is still very fast. Since in Dynamic Logic gates the inverter connects to only nFETs , it too is very fast. Secondly the size of pFET in an inverter can be made smaller than in some types of logic gates(**Abdel-Hafeez** and **Ranjan** et al 2001).Dynamic logic is widely used in high performance microprocessors and is attractive for high speed circuits.

2.1 DYNAMIC LOGIC

In high density, high performance digital implementations where reduction of circuit delay and silicon area is a major objective, dynamic logic circuits offer several significant advantages over static logic circuits (**S.M.Kang** et al 1999; **A.K.Pandey** et al 2012).Dynamic circuit uses a clocked pull up transistor rather than a pMOS that is always ON (**N.H.E.Weste** et al 2005). Fig2.1a shows a generalised CMOS dynamic logic circuit (**Charles F.Hawkins** et al 2004). The operation of all dynamic logic gates depends upon on temporary storage of charge in parasitic capacitance. (**Jan.M.Rabaey** et al 2002). The circuit is based on first precharging the output node capacitance and subsequently, evaluating the output level according to the applied inputs.



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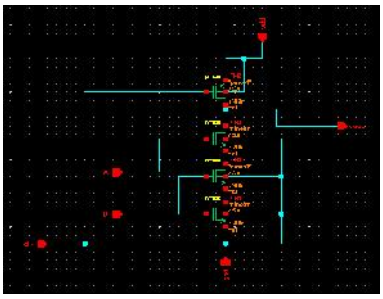


Fig 2.1a: DYNAMIC LOGIC CIRCUIT AND SCHEMATIC.

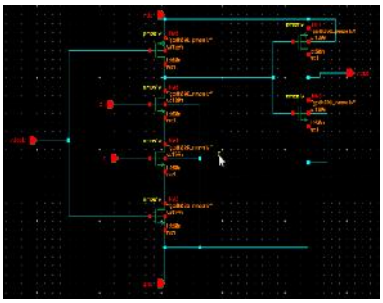
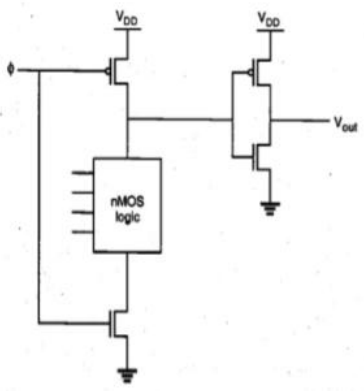


Fig 2.2a : DOMINO LOGIC CIRCUIT AND SCHEMATIC

2.2. DOMINO LOGIC

Domino circuits are widely used in high-speed applications for the implementation of high fan-in circuits (**V. De and S. Borkar** et al 1999**)**. However, domino circuits are vulnerable to noise. The noise sensitivity of domino circuits is due to their low switching threshold voltage, which is equal to the threshold voltage of NMOS devices in the evaluation network. The substantial increase in deep-submicron noise with technology scaling severely impacts the usefulness of domino circuits (**M. Anders** et al 2001**; F.Mendoza et al**). With technology scaling, the supply voltage is scaled down to decrease the power consumption. In order to improve performance, the transistor threshold voltage has to be commensurately scaled to maintain a high drive current. However, the threshold voltage scaling results in the substantial increase of the sub threshold leakage current (K **. Roy, S. Mukhopadhyay** et al 2002). The main source of noise in deep-submicron circuits is mainly due to the high leakage current, crosstalk noise, supply noise, and charge-sharing (**C. H. Cheng** et al 1999; **Ashutosh Bhardwaj** et al). As the technology scales down, the leakage of the evaluation transistors exponentially increases due to lower threshold voltage.



Features of Domino Logic

- They have smaller areas than conventional CMOS logic (as does all Dynamic Logic).
- Operation is free of glitches as each gate can make only one transition.
- Only non-inverting structures are possible because of the presence of inverting buffer.
- Charge distribution may be a problem.

2.3 PSEUDO DOMINO BUFFER LOGIC

The previous section illustrates the issue of performance degradation due to the propagation of the pre-charge pulse inherent in domino logic gates . The PDB-based implementation over comes this problem using the circuit structure shown in Fig 2.3a **(T. Fang, B. Amine, G. Zhouye** 2012). In this implementation of the buffer, the source of the buffer's NMOS transistor M5 is connected to node B instead of Gnd. Using the propagation of the pre-charge pulse from node Z through the static buffer results in increased power consumption. In addition, the output logic is unstable during the pre-charge phase and as a result the cascading performance is limited such a circuit topology , the value at node Z cannot propagate to the output F during the precharge phase of the gate since during this phase, the evaluation transistor M2 is turned off .For our proposed gate, when the input logic A is low, the floating node Z is always high and then, the output node F is kept low regardless of the operating phase. On the other hand, if the input A is high, the pre-charge and evaluation phases will lead to the following situation. During the evaluation phase, node Z is discharged to Gnd as well as node B, resulting in enabling the PMOS transistor M4, while pulling up the output F to Vdd. During the pre-charge phase node Z is charged up to Vdd, followed by the voltage at node B. Since the NMOS evaluation transistor M2 is disabled the output node

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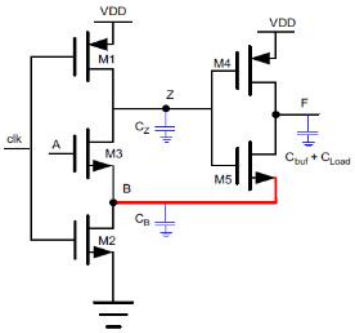
Z is held high. It is important to note that during the pre-charge phase, the output node F is isolated from Gnd. In other words the pre-charge pulse at node Z cannot propagate through the buffer to the output node F.



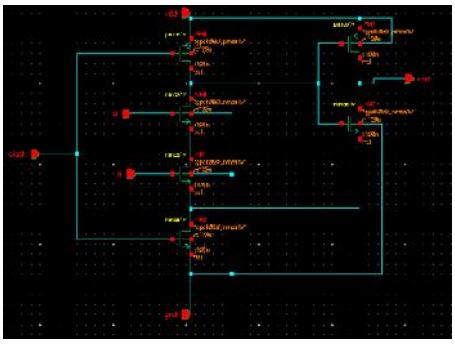
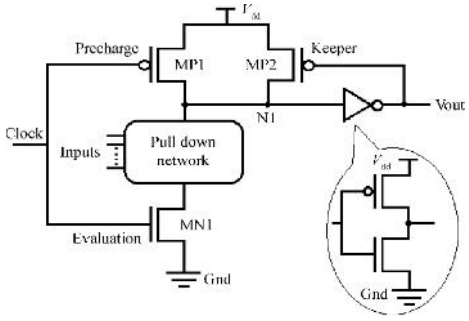


Fig 2.3a: PSEUDO DOMINO BUFFER LOGIC CIRCUIT AND SCHEMATIC

2.4 KEEPER DOMINO LOGIC

Traditionally, dynamic floating nodes have been avoided by employing a static path through a pull-up and/or pull-down device referred to as a "keeper"(**A. Alvandpour** et al 2002) For small leakage currents, weak keepers were sufficient to maintain the voltage level of precharged nodes without a significant impact on the performance of the dynamic gates. However, in the presence of increasingly larger leakage currents, the keepers must be sized to compensate for these leakage currents, which significantly degrade the performance of dynamic circuits due to contention.



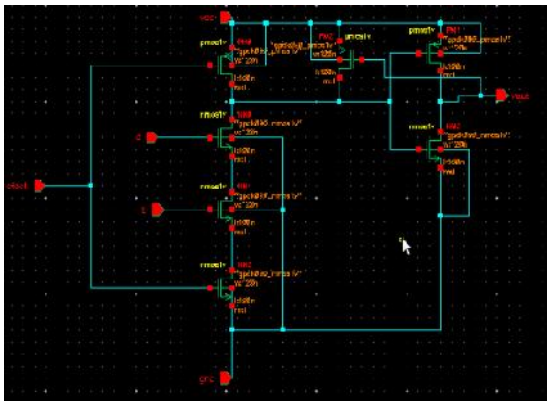
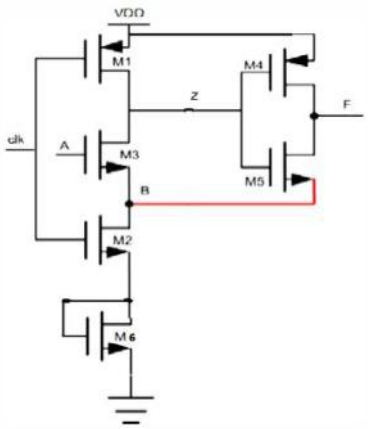


Fig 2.4a : KEEPER DOMINO LOGIC CIRCUIT AND SCHEMATIC

2.5 FOOTED DIODE DOMINO LOGIC

Performance degraded in a domino circuit is due to propagation of pre-charge pulse from dynamic node to the output node. The PDB based design for domino logic compensates this problem up to some extent (**P. Ali, Asyaei** et al 2012**)** but there is always a room for improvement. In our proposed circuit we put an NMOS transistor which is working as a diode in between GND and M2 clock transistor (**H.Mahmoodi-meimand and K. Roy** et al 2004). Let us take an example of a diode footed buffer shown in the fig 2.5a. In the circuit shown the source of the NMOS transistor m5 is connected to the node B instead of the GND. An NMOS transistor is introduced in the circuit whose gate is shorted with its drain and connected to the source of the NMOS clock transistor M2, the source of NMOS transistor M6 is connected to ground. In the circuit when input A is low then dynamic node Z is always high and output is kept low regardless of operating phase.



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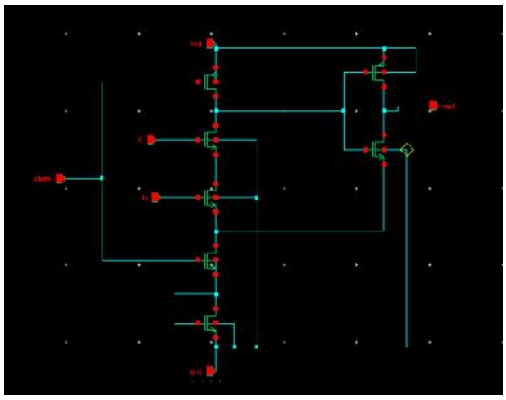

Fig 2.5a : FOOTED DIODE DOMINO LOGIC CIRCUIT AND SCHEMATIC

3 RESULTS AND ANALYSIS

The designs using different logics are tested on cadence tool using 180nm and 90nm technology files. Table 3.1a, 3.1c shows the results of 180nm and 90 nm technology and 3.1b, 3.1d graphically shows the same.

Logic	Delay	Power	PDP
Dynamic	4.50E-6	2.798E-6	12.55E-12
Domino	3.076E-6	5.049E-6	15.53E-12
Keeper Domino	4.753E-6	3.673E-6	17.464E-12
Pseudo Domino Buffer	6.002E-6	1.857E-6	11.15E-12
Footed Diode Domino	6.009E-6	1.431E-6	8.599E-12

Table 3.1a : RESULTS USING 180NM TECHNOLOGY.

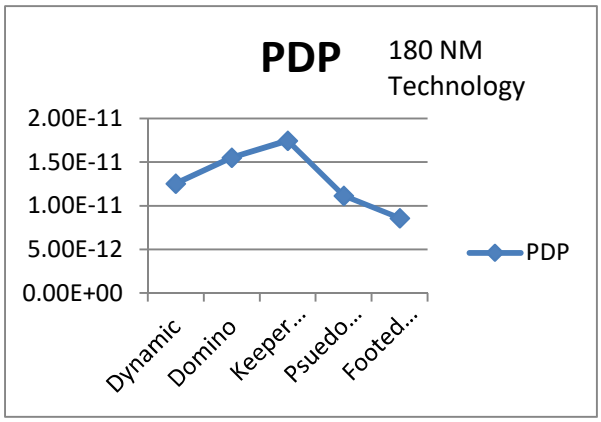

Fig 3.1b : PDP RESULTS USING 180NM TECHNOLOGY.

Logic	Delay	Power	PDP
Dynamic	4.50E-6	879E-9	3.959E-12
Domino	3.075E-6	2.988E-6	9.173E-12
Keeper Domino	4.754E-6	1.30E-6	6.209E-12
Pseudo Domino Buffer	6.003E-6	1.618E-6	9.713E-12
Footed Diode Domino	6.009E-6	654E-9	3.93E-12

Table 3.1c : RESULTS USING 90NM TECHNOLOGY.

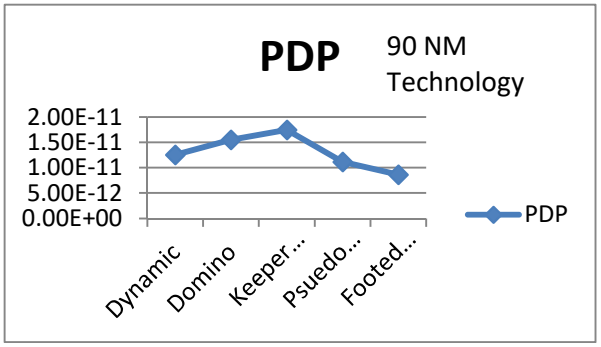

Fig 3.1d : PDP RESULTS USING 90NM TECHNOLOGY

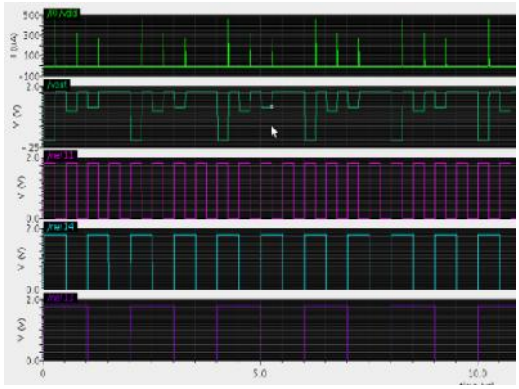

Fig 3.1e : ANALYSIS OF DYNAMIC NAND

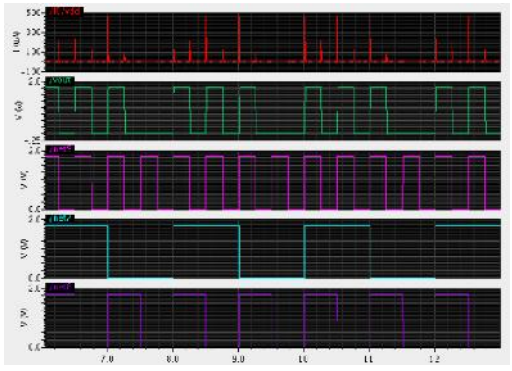

Fig 3.1f : ANALYSIS OF DOMINO NAND

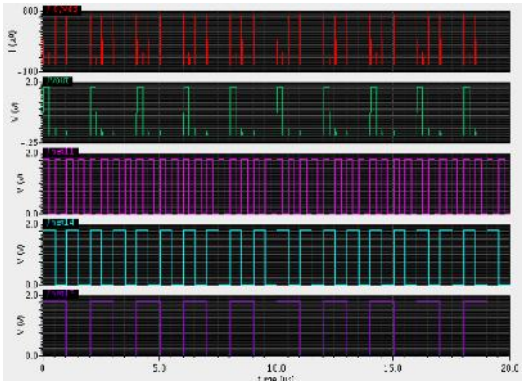

Fig 3.1g: ANALYSIS OF KEEPER DOMINO NAND

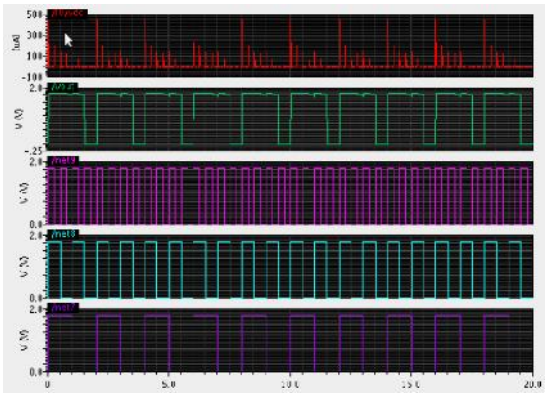

Fig 3.1h : ANALYSIS OF PSEUDO BUFFER DOMINO NAND

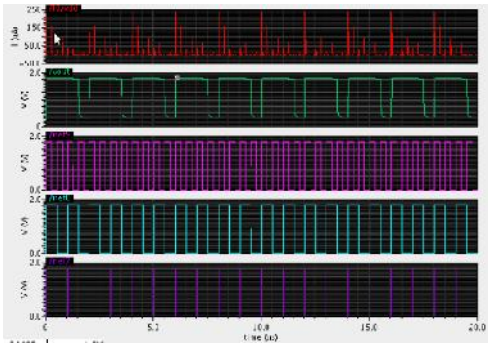

Fig 3.1g : ANALYSIS OF FOOTED DIODE DOMINO NAND

4 CONCLUSIONS AND FUTURE WORK

With the energy saving Footed Diode Domino or Pseudo Domino Buffer logic the energy consumed in a circuit can be minimised. Depending upon the system requirements and application these logics may be used to design ultra low power circuits. This work shall be further carried out on bigger circuits like multiplexer and then to barrel shifter for further optimisation power, delay and area.

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