International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 8
August 2017

Academic Science

Design of SRAM Array using Reversible Logic for Low Power Non-volatile applications

Hamsa S
Research Scholar, Jain University
Basavaraj H
Research Scholar, Jain University
Ananth A G
NMAM Institute of Technology, NITTE, Udupi

ABSTRACT:
With the advancement in technology and type of usage of the electronics devices in different applications, demands huge size memories to store or process the data. Typically, Static Random Access Memory (SRAM) cells are used due to its high-speed access characteristics. One of the primary applications of SRAM is that is used as Cache memory which is exceptionally fast which will speed up the task of processor. A single SRAM cell, 32x32 SRAM memory array in reversible logic, decoder circuit, read/write drivers and sense amplifiers are designed and verified using Cadence. Reversible circuits in recent years have gained its interest due to its low power characteristics. A novel SRAM cell design using reversible logic is proposed. The proposed design minimizes the Quantum delay by approximately 30% and the power by approximately 35% than the existing designs.

Keywords: Reversible logic, SRAM

I. INTRODUCTION

With advancing technology, there is always a greater demand for larger, faster and nonvolatile data storage devices. This has driven the fabrication technology and memory development towards more compact design rules. A variety of memories are available to store and access the information, according to ones need one may select a read only memory or a read write memory as per the required applications. Although SRAM requires more space, it is easily fabricated, doesn't require refresh circuit and is much faster. Hence for SRAMs the standby power is very low despite of high density of transistors. SRAM cells have better noise immunity due to larger noise margins, and have ability to operate at low power supplies.

The advantage of 6T cell is that static power dissipation is very less; essentially, it is limited by the PMOS transistors. With the exponential increase in the size of the memory, the power consumed by the memory cells is also increasing exponentially. Using CMOS logic, the SRAM is operated with 0 to 1v, 1v supply voltage and consumes 44.76 µW. The SRAM is designed and Implemented in standard 45nm technology using Cadence Virtuoso tool for schematic. To improve the power dissipation, delay factors and area, we make use of another logic called "REVERSIBLE LOGIC" that has few advantages when compared with CMOS logic.

II. REVERSIBLE LOGIC

"Reversible Logic" circuit takes n-inputs and gives n-outputs. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments. SRAM uses a simple bi-stable circuit to hold a data bit. Two cross coupled inverters in the conventional 6T cell forms a latch which is used to store the data. Whenever there is a need for

storing other data in the same cell, previous data has to be erased which proves the irreversibility operation of the memory cell and results in the heat dissipation, hence SRAM is designed using reversible circuit.

A circuit is reversible if it maps each input vector into a unique output vector and vice versa. The gate which does not lose any information is called as reversible gate. Reversible circuit has gained its interest due to its minimization of non-adiabatic losses which will reduce the heat dissipation. With the increase in the memory application, designing of low power memory cell has gained interest in recent years.

The reversible logic operations do not wipe away (lose) information and dissipates lesser amount of heat. Thus, reversible logic is probable to be in demand in high speed power conscious circuits. Reversible circuits are of high importance in low-power CMOS design, optical computing, quantum computing and nanotechnology. The most major application of reversible logic lies in quantum computers. A quantum computer can be viewed as a quantum network composed of quantum logic gates or circuits; each gate performs an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

III. TYPES OF REVERSIBLE LOGIC GATES

Feynman Gate

Fig 1 shows the schematic of 2 input and 2 output Feynman gate. The inputs are A and B, the outputs are Y1 and Y2, where Y1 follows A and Y2 gives A xor B. The quantum cost of a Feynman gate is 1.

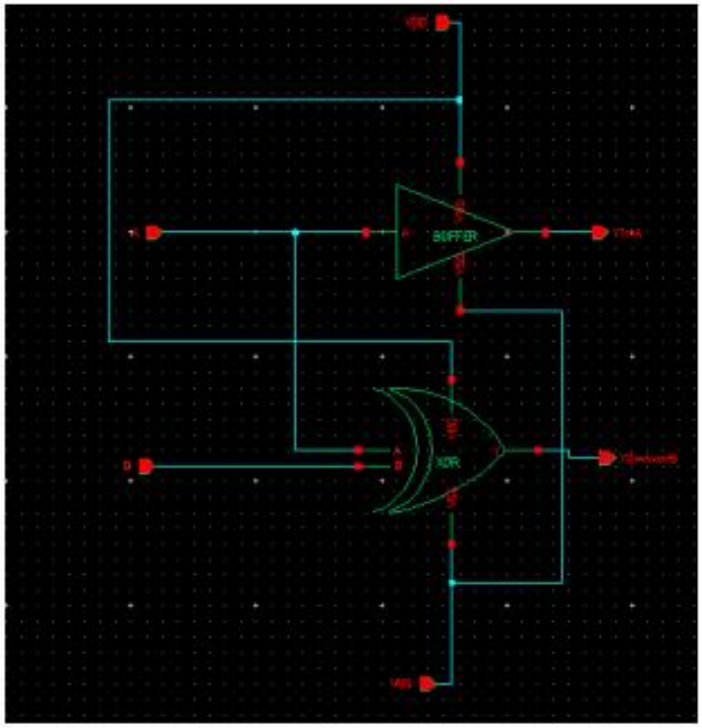

Fig 1: Schematic of Feynman Gate

Toffoli Gate: Toffoli gate is a 3 input, 3 output reversible logic gate. The inputs are A, B and C, the outputs P,Q and R. The outputs P, Q and R are related to inputs as P=A, Q=B, R=AB +C. The quantum cost of a Toffoli gate is 5.

International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 8
August 2017

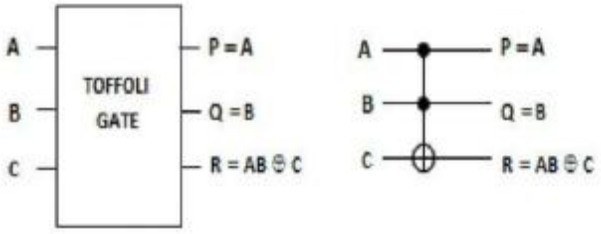

Fig 2: Toffoli Gate[5]

Fredkin Gate: Fredkin gate is 3 input, 3 outputs reversible logic gate. The inputs are A,B and C, the outputs are Y1, Y2 and Y3. The outputs are related inputs as Y1=A, Y2= A' B+AC and Y3= A'C+AB. The quantum cost of a Fredkin gate is 5.

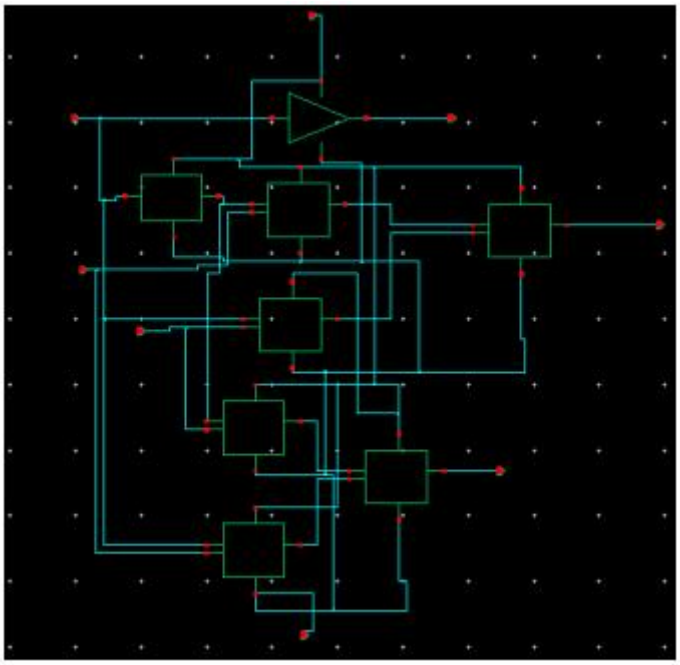

Fig 3: Schematic of Fredkin Gate

Peres Gate: Peres gate is a 3 input, 3 output reversible logic gate. The inputs are A,B and C, the output vector comprises of (P, Q, R). The output is related to inputs as P = A, Q = A+B and R=AB +C. The quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

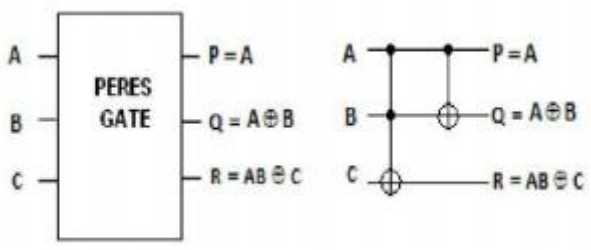

Fig 4: Peres Gate[5]

International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 8
August 2017

IV. DESIGN AND IMPLEMENTATION

SRAM Cell

A single SRAM cell was modelled by using one Feynman gate and one Fredkin gate. Word-line (WL) output in 3×3 Fredkin gate is used to enable the row cells. So, the total number of garbage output for the proposed SRAM cell is 1. Considering the line 2, if WL = 0, data stored will be the output in line 2 of the 3 × 3 Fredkin gate which resembles the hold state of the access transistor. If WL = 1, data input will be the output of the line 2. This line 2 is fed to the Feynman gate which performs the latch operation.

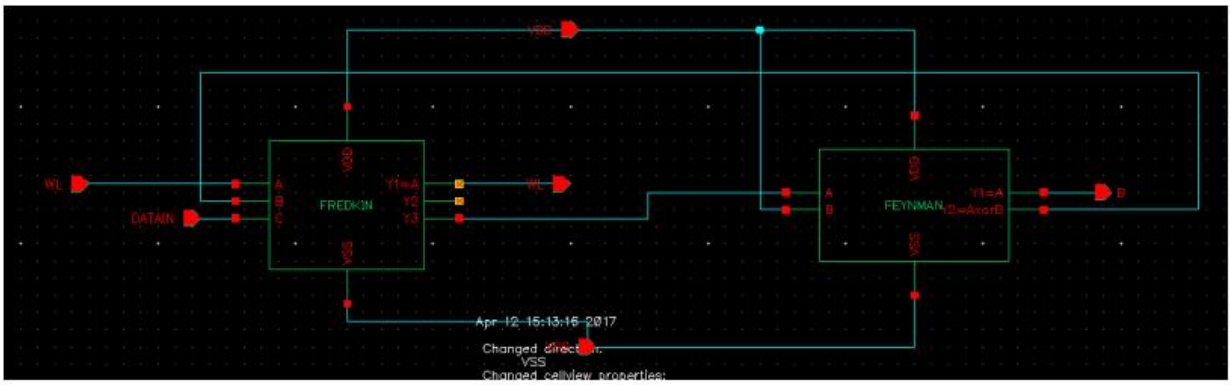

Fig 5: Schematic of SRAM Cell

SRAM cell with read and write circuit

This section discusses about the proposed reversible SRAM cell with read and writes signals. A 3 × 3 Fredkin gate and a 2 × 2 Feynman gate is used to store the single bit of data and it is controlled by two 3 × 3 Fredkin gate. The input to the SRAM cell is word line signal from the row decoder, write signal, data in, read signal and the output of the SRAM cell is write line which is passed to the next SRAM cell in the same row, write line, read line and data out.

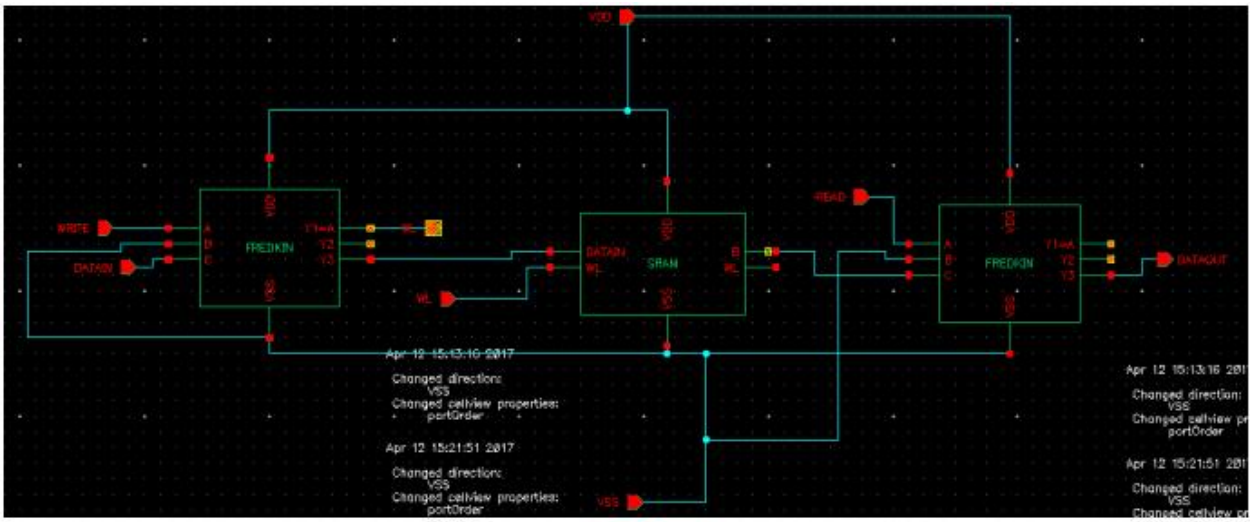

Fig 6: Schematic of SRAM read/write logic

32x32 SRAM Cell

In this section, 32x32 SRAM array was proposed. The decoder is used to translate the input address and is used to select the appropriate word lines. The word line output of each SRAM cell is used to enable the next SRAM cell there by reducing the garbage output of each SRAM cell. The input data was given by the write circuits and the bit and bit of each SRAM cell is connected to the sense circuits in order to perform the read

operation. In the proposed SRAM array, eight 2-to-4 decoders are used with enable bit to connect eight reversible SRAM cells in an array.

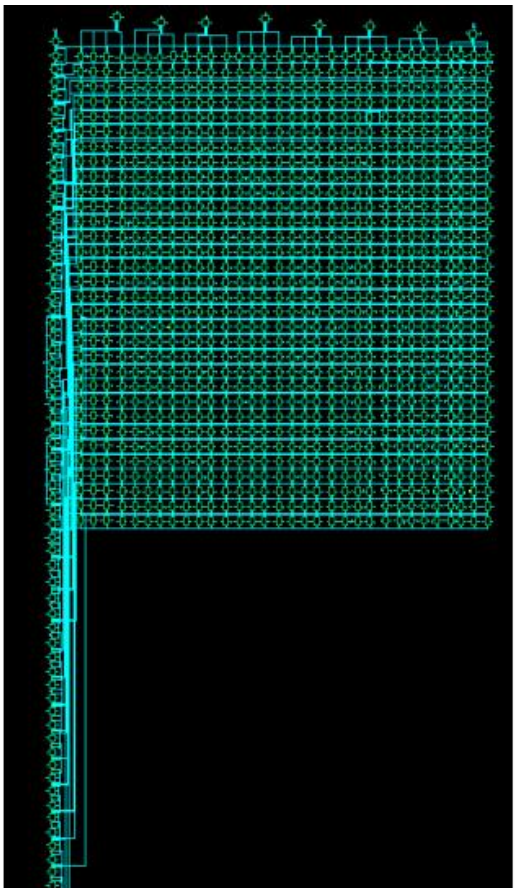

Fig 7: Schematic of 32x32 SRAM

V. RESULTS AND DISCUSSIONS

Power consumption and Delay

Power Consumption is an important parameter in the designing of SRAM chip. It plays a vital role in deciding the components based on its values. Power Consumption is calculated for the circuits used in the design and listed below.

Table 1: Table of Results

Sl. No	Circuit	Power	Delay
1	Decoder 2:4	30.26µW	299.2ps
2	Feynman gate	6.54µW	103.7ps
3	Fredkin gate	16.91µW	50.46ns
4	SRAM cell	50.3nW	40.58ns
5	SRAM read/write	2.68mW	40.99ns
6	Overall power and delay	2.733nW	132.3ps

VI. CONCLUSION

A novel 32x32 SRAM cell was proposed in Reversible logic using Fredkin and Feynman gates. The Complete array which includes peripheral components such as memory cell, driver circuit, column and row decoder circuits, read and write circuit designed and integrated with the cadence software. The proposed work is operated with 0 to 1v, 1v supply voltage and consumes 2.733nW power. The SRAM is designed and implemented in using Cadence Virtuoso tool for schematic. The worst case delay of the proposed SRAM cell is approximately 30% lesser than the design of SRAM cell using CMOS circuit design. The circuit was optimized and the number of garbage outputs are reduced to 1 which lesser than the existing reversible SRAM cell.

VII. REFERENCES

[1] K. Dhanumjaya, M. Sudha, Dr.MN.Giri Prasad, Dr.K.Padmaraju, "Design of Low Power SRAM in 45nm CMOS Technology", IJERA, vol.1, Issue 4, pp. 2040-2045, 2014.

[2] Prateek Asthana et.al, "Performance Comparison Of 4T, 3T AND 3T1D DRAM Cell Design on 32nm Technology", JSSATE, ICCSEA, SPPR, VLSI, WiMoA, SCAI, CNSA, WeST - 2014, pp. 121–133, 2014.

[3] K. Dhanumjaya, M. Sudha, Dr.MN.Giri Prasad, Dr.K.Padmaraju, "Cell Stability Analysis Of Conventional 6t Dynamic 8t SRAM Cell In 45nm Technology" International Journal of VLSI design & Communication Systems (VLSICS) vol.3, No.2, April 2012

[4] M. Morrison, M. Lewandowski, R. Meana, and N. Ranganathan, "Design of static and dynamic ram arrays using a novel reversible logic gate and decoder," in Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on, Aug 2011, pp. 417–420.

[5] Prashant .R.Yelekar, Sujata S. Chiwande, " Introduction to Reversible Logic Gates & its Application" *2nd National Conference on Information and Communication Technology (NCICT) 2011*

[6] V. Gupta and M. Anis, "Statistical design of the 6T SRAM bit cell," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 1, pp. 93–104, Mar. 2010.

[7] S. Mahammad and K. Veezhinathan, "Constructing online testable circuits using reversible logic," Instrumentation and Measurement, IEEE Transactions on, vol. 59, no. 1, pp. 101–109, Jan 2010.

[8] David Choi, Kyu Choi, and John D. Villasenor, "New Non-Volatile Memory Structures for FPGA architectures", IEEE transactions on Very Large Scale Integration (VLSI) systems, Vol. 16, no. 7, July 2008.

[9] E. Fredkin and T. Toffoli, "Conservative logic," in Collision-Based Computing, A. Adamatzky, Ed. Springer London, 2002, pp. 47–81

[10] Jeffrey Dreibelbis, "Introduction to the Memory Section", IEEE Journal of Solid-State Circuits, vol. 33, no. 11, November 1998

[11] C. Bennett, "Logical reversibility of computation," IBM Journal of Research and Development, vol. 17, no. 6, pp. 525–532, Nov 1973.

[12] R. Keyes and R. Landauer, "Minimal energy dissipation in logic," IBM Journal of Research and Development, vol. 14, no. 2, pp. 152–157, March 1970.

[13] R. Landauer, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 5, no. 3, pp.183–191, July 1961.