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Design and Characterisation of Low Power Folded-Cascode Operational Amplifier

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ABSTRACT:

The trend towards low voltage low power silicon chip systems has been growing rapidly due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The supply voltage is being scaled down to reduce overall power consumption of the system.

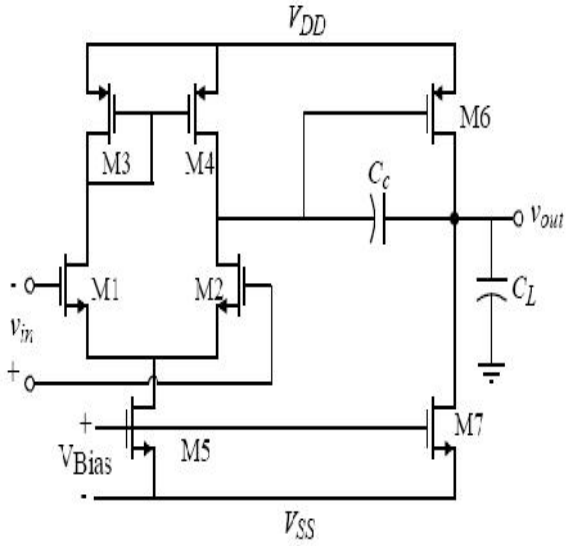
This paper presents a design of the Folded-cascode operational amplifier using 180nm CMOS technology, The objective of this project is to, Study basic design of operational amplifier, Implement the full custom design of low voltage and low power folded cascode operational amplifier and Improves the Slew Rate, Bandwidth, Gain & PSRR of op-amp which can be used for analog to digital converter (ADC) as well as digital to analog converter (DAC) applications.

Keywords: Folded-Cascode operational amplifiers, CMOS, MOSFET, PSRR, Gain, Bandwidth, Slew rate.

I .INTRODUCTION:

Improvements in processing have pushed scaling of device dimensions persistently over the past years. The main drive behind this trend is the resulting reduction in IC production cost since more components on a chip are possible. In addition to device scaling, the increase in the portable electronics market is also encouraging low voltage and low power circuitry since this would reduce battery size and weight and enable longer battery life time. Operational amplifier, which has become one of the most versatile and important building blocks in analog circuit design. An Operational amplifier is basically a multistage amplifier in which a number of amplifier stages are interconnected to each other. Its internal circuit consists of many transistors, FETs and resistors. An op-amp is a DC-coupled voltage amplifier with a very high voltage gain.

Our goal is the design analysis and simulation of a Low voltage Folded-Cascode Op Amp using CMOS process in order to use it in wide applications like in the design of, analog-to-digital (A/D)as well as digital-to-analog (D/A) converters, input and output signal buffers, and many more, and to compare its some of the performance parameters with the two-stage op-amp by designing cascode op-amp for the almost same specifications.



Circuit of two stage op-amp:

Two-stage OP-AMP mainly consists of a cascade of Voltage to Current and Current to voltage stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load recovering the differential voltage. The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. The second stage is also nothing more than the current sink inverter.*Circuit of Folded Cascode op-amp:*

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Folded cascode architecture was developed in part to improve the input common mode range and the power supply rejection of the two stage operational amplifier. The folded cascade op amp uses cascoding in the output stage combined with a differential amplifier to achieve good input common mode range. This op amp offers self compensation, good input common mode range and improves gain of two stage op amp.

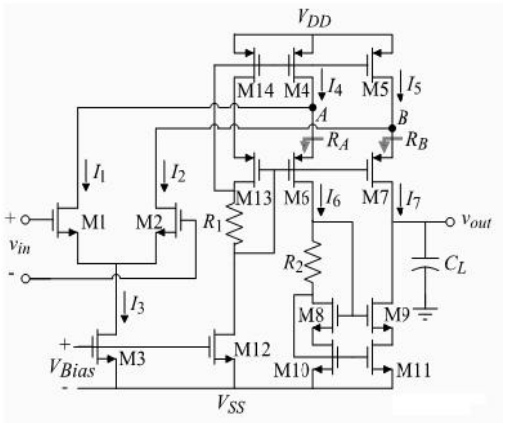

Fig 2: Folded cascade Op-Amp circuit diagram

II. LITERATURE SURVEY:

Paper[1]"A Novel class of complementary folded-cascode op-amps for low voltage" presented by Falk Roewer and Ulrich Kleine in August 2002. Three novel structures of complementary folded cascode op amps with rail-to-rail input capability were presented.This op-amps have been fabricated with a standard 0.8um CMOS technology.This op--amps provides low voltage capability, high bandwidth due to minimum internal nodes.

Paper[2] "Design of High Gain Folded-Cascode Operational Amplifier Using 1.25 um CMOS Technology" prsented by Dr. Rajni in November-2011. Folded-Cascode op-amp provides a high output resistance which leads to high gain as compared to a normal cascode circuit. Described a comparison between the cascode and Folded-Cascode op-amps.A design of the Folded-cascode op-amp have been fabricated using 1.25µm CMOS technology.

Paper[3]"Design of 1v, 0.18µm Folded cascode operational amplifier for switch Capacitor sigma delta modulator"Presented by Ratnaprabha w. Jasutkar, P. R. Bajaj & A. Y. Deshmukh in Oct 2013. The folded cascode Op-amp gives highest unity gain bandwidth which is nearly double the simple cascode Op-amp.This paper presents the folded cascode op-amp which is to be used in switch capacitor sigma delta modulator.A design of the Folded-cascode op-amp have been fabricated using 0.18µm CMOS technology.

III. METHODOLOY:

Design of the folded cascade operational amplifier consists of determining the specifications, selecting device sizes (W/L) and biasing conditions, compensating the op amp for stability, simulating and characterizing the op amp Aol (open-loop gain), CMR (common mode range on input), CMRR (common mode rejection ratio) and PSRR (power supply rejection ratio).

Design Equations to be used for folded cascade op-amp:-

Slew rate I3=SR.CL

Bias currents in output cascades, avoiding zero currents in cascades

I4=I5=1.2I3 to 1.5 I3

Maximum Output Voltage,

Vout(max)Vsd(sat)=Vsd7(sat)=(VDD-Vout(max))/2

Minimum output voltage.Vout(min)

Vds9(sat)=Vds11(sat)=(Vout(min)-|Vss|)

Self-bias cascode

R1=Vsd13(sat)/I12 and R2=Vds8(sat)/I6

GB=gm1/CL

Power dissipation(Pdiss)=

(VDD-Vss)(I3+I12+I10=I11)

Design Equation to be used for folded cascade op-amp:-

Determine the necessary open-loop gain (Ao)

gm1 = gm2 = gmI, gm6 = gmII, gds2 + gds4 = GI, and gds6 + gds7 = GII

Slew Rate = I5/Cc

First-Stage Gain Av1 = (-gm1)/(gds2+gds4) = (-2gm1)/[I5(λ2+λ4)]

Second -Stage Gain Av2 = (-gm6)/(gds6+gds7) = (-gm6)/[I6(λ6+λ7)]

Gain bandwidth GB = gm1/Cc

Output pole p2 = -gm6/CL

RHP zero z1 = gm6/Cc

The desired design Specifications of two stage op-amp as well as folded cascode op-amp are:

Specifications	Values
Technology	180nm
Power supply	1.8V
Gain	100dB
Bais current	20uA
Load capacitance	2pF
Slew rate	10V/usec
Unity Gain bandwidth	500MHz
Power consumption	<1mW
PSRR	>60dB

IV. CONCLUSION:

This paper research of the Folded-cascode amplifier using 180 nm CMOS technology. Initially our work will describes the design of two-stage op amp using the same i.e. 180nm technology and then to overcome some of the limitations of the two stage op amp. we will design a low power folded-cascode op amp which improves the Slew Rate, Bandwidth, Gain & PSRR of op-amp which can be used for analog to digital converter (ADC) as well as digital to analog converter (DAC) applications.

REFERENCES:

[1] Falk Roewer and Ulrich Kleine, "A Novel class of complementary folded-cascode op amps for low voltage" , IEEE Journal of Solid-State Circuits, Vol. 37, no. 8, August 2002.

[2] Er. Rajni,"Design of High Gain Folded-Cascode Operational Amplifier Using 1.25 um CMOS Technology" , International Journal of Scientific & Engineering Research Volume 2, Issue 11, November-2011.

[3] Ratnaprabha w. Jasutkar, P. R. Bajaj & A. Y. Deshmukh, "Design of 1v, 0.18µ Folded cascode operational amplifier for switch Capacitor sigma delta modulator", International Journal of Electrical and Electronics Engineering Research (IJEEER) Vol. 3, Issue 4, Oct 2013.

[4] Jalpa solanki,"Design and Implementation of High Gain, High Bandwidth CMOS Folded cascode Operational Transconductance Amplifier", 2014 IJEDR Volume 2, Issue 1 ISSN: 2321-9939.

[5] Suparshya Babu Sukhavasi,Susrutha Babu Sukhavasi, Dr. Habibulla khan "Design of a Low Power Operational Amplifier by Compensating the Input Stage", Vol. 2, Issue 2, Mar-Apr 2012, pp.1283-1287

[6].P. E. Allen, D. R. Holdberg "CMOS Operational Amplifiers," in CMOS Analog Circuit Design, 2nd ed. New York, USA: Oxford Univ. Press,2002

[7]H. Daoud, S. Ben Salem, S. Zouari, M. Loulou, "Folded Cascode OTADesign for Wide Band Applications," International Conference on Design and Test of Integrated Systems in Nanoscale Technology, 2006.

[8]P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, "Operational Amplifiers with Single-Ended Outputs," in Analysis and Design of Analog Integrated Circuits, 5th ed. USA: Wiley, 2009, ch. 6, sec. 6.6, pp. 442-446