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Implementation and Power Analysis of 32-bit MIPS-based CPU on Xilinx FPGAs

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ABSTRACT

The aim of this paper is, to introduce design of a 32-bit MIPS (Microprocessor Interlocked Pipeline Stages) based processor containing five stages of pipeline, to incorporate power optimization techniques for FPGAs. The functionality of this design has been verified by writing Verilog Modules on Xilinx 14.5 selecting the target FPGA device. The design helps to improve the speed and increase the whole throughput of the processor. Synthesis and simulation results have been taken from ModelSim 6.2c. Analysis the design floorplan of 32-bit CPU and study of the detailed netlist has been performed on PlanAhead tool, which was giving accurate results. From the performance viewpoint, FPGA-based implementation of processor is totally centered on the designing of processor architectures in Verilog HDL and increasing the overall speedup with power mitigation at Spartan class (45nm and 90nm) FPGAs. The significant features of this work are; increased number of instructions, enhanced performance and low power consumption with HDL modification techniques. The design has 5 levels of logic and delay of 14.202ns with the maximum frequency of operation at 70.413MHz for Spartan-6. Optimized power observed was about 22.72% after applying power reduction techniques, which make this work useful for low power FPGAs.

Keywords

MIPS, CPU, FPGA, Verilog, ModelSim, HDL modification techniques, Power Reduction

INTRODUCTION

High-performance electronic devices releasing a large amount of heat inflict practical limitation on how far can we enhance the performance of the system. Field Programmable Gate Arrays gives time to market quickly and the re-programmability feature usually makes them the important part of the system. It can be used to implement an entire System-On-Chip (SOC). To implement a complex design like CPU system using top-down approach, the design has divided into small sub-functions which has been implemented using one logic block. Programming interconnects are the reason behind the connected sub-functions in logic blocks [21].

In 1980's, a research development on the MIPS architecture was introduced at Stanford University. The corporation was originated in 1984 to industrialize this research. Though, various companies create processor chips following MIPS-based architecture, with taking LSI logic, Philips, Toshiba NEC and NKK. This MIPS design is a quarter of a century old, its chips are generally used in present systems such as CISCO Routers, other embedded applications including set-top boxes for digital TV, cable modems and DVD recorders. Because of its clean and simple architecture, it is very convenient for designers. A series of evolution has been evolved for this architecture branded as; MIPS-I, II, III and IV. Each ISA is an advanced version of the former one. That's why we can say that all the features found in MIPS-I, are also located in II, III and IV. Earlier MIPS i.e. I and II instruction set architectures were 32-bit architectures, 64-bit capabilities were added in MIPS-III with a subset of core 32-bit and architecture IV expanded this [19].

Today, the increased complexities in real-time application have high power requirements. That computational power can accomplish by high performance components as RISC or CISC microprocessors and non-programmable chips like ASICs and FPGAs. Mostly, to upgrade the speed

and performance of the system, algorithms are needed which can compute at low running time complexity. Secondary way to increase the performance is designing a high speed VLSI chip for such systems. Yet, current processor designs are more concerned with exhibiting multi-stage pipeline power for quick execution. To demonstrate the target FPGA, it is very useful for real time operating systems.

Nowadays, FPGA and other electronic devices need to be realized with power optimization methods because of power consumption and area. An integrated flow provided by Xilinx ISE with the Model Technology, ModelSim Simulator, allows the user to run simulation from the Xilinx Project Navigator. Obtaining dynamic power reduction goals in Spartan-6 and Spartan-3 using HDL modification was a challenging task. Static power increases with transistor size shrink; it is ruled by transistor leakage current. Dynamic power was the matter of interest at 45nm and 90nm CMOS technologies [18].

OVERVIEW

This section discusses the previous related work done on RISC processors. Low power techniques have been used related to RISC processor design including Clock gating, Power gating, Multi-Voltage gating, etc. Soumya Murthy, UshaVerma has introduced a low power reduction technique to design DLX based CPU using HDL modification [1]. In this method, Verilog HDL coding styles were used to minimize power for Xilinx FPGA. Although the dynamic power was optimized up to 13.33% but it has increased the overall path delay. S.P. Ritupurkar, M.N. Thakare, G.D. Korde presented the RISC CPU based on MIPS using VHDL [2]. It described the instruction set, architecture and timing diagram of processor and achieved reduced delay at 1.35GHz at the cost of high power consumption. Neenu Joseph, Sabarinath S has proposed a method of clock gating to reduce power. The major disadvantage for this technique is, the control logic for the clock gating increases the design area requirements [3]. Pranjali S. Kelgaonkar, Prof. ShilpaKodgire [4] has designed 32-bit Pipelined RISC on Spartan-6 including five stage pipelined RISC CPU and implemented ALU block on Spartan-6 using Xilinx. According to the literature survey, dynamic power has been reduced at different levels of design. In this paper, we have optimized the dynamic power on MIPS architecture by taking different FPGAs using HDL modification technique which is giving better results.

RISC PROCESSOR SPECIFICATIONS

This 32-bit RISC processor with five stage pipeline has the following key concepts:

1. MIPS 32-bit processor instruction set architecture, which has R-type, I-type and J-type instruction formats.

2. It consists of 32-bit wide program counter and a bank of 32 general purpose registers of 32-bit.

3. It has 32-bit address and data lines to execute any ALU operation.

4. Five stage pipeline registers: fetch, decode, execute, memory-access and write back. Better performance and throughput due to pipelined MIPS architecture designed using Verilog HDL.

5. Synthesizable code designed in Xilinx ISE for all compatible FPGA devices like Spartan-3E, Spartan-3A, Spartan-6, Virtex-5, Virtex-6, etc.

6. Power optimization at architecture and design level resulting in low power consumption.

7. Simulation results are clearly showing the proper execution of instructions.

The majority of microprocessor designs start with specifying what the microprocessor is expected to be able to do, which is translated into its ISA. Instruction Set Architecture (ISA) defines the microprocessor from a machine-language programming perspective, including the following:

- ✓ Instruction set

- ✓ Structure of the register file
- ✓ Addressing modes
- ✓ Data types and data representation
- ✓ Run-time operations (exceptions for instance)

A top-down approach has been followed to illustrate the system and CPU architectures highlighting their sub-components. A CPU instruction format is a single 32-bit aligned word.

1. Immediate
2. Jump
3. Register

Immediate Instructions; it is also possible to alert a constant as one of the two operands. The constant is coded into the instruction as a 16-bit integer; hence, it must remain in the range of -32678 ≤ constant ≤ 32767 for addi, addiu, slti or 0 ≤ constant ≤ 65535 for andi, ori, xori. The constant is converted into a 32-bit value either by filling the upper 16 bits with a copy of the sign bit i.e. addi, addiu, slti, sltiu or with 0's i.e. andi, ori, xori [8].

The branch instructions; They have 16 bits for encoding a target address, comparative to the current instruction, making most of memory from any given location. Though, There are times, when it is necessary to transfer control to an arbitrary location [8].

R-type instructions involve arithmetic, logical, and shift operations on MIPS, which encode the operation to be executed and three general registers- Rs, Rt and Rd. It is predictable, in MIPS documentation, to refer to the two source registers as Rs and Rt, and one destination register as rd. Each of them is actually encoded in the instruction as a 5-bit integer that specifies one of the 32 general registers [8].

32-BIT RISC PIPELINED ARCHITECTURE

Pipeline improves instruction throughput instead of individual instruction execution time. The processor which has been designed is divided into five pipeline stages. The five pipelined stages are fetch, decode, execute, memory and write-back. Since, each stage has only one-fifth of the whole logic, the clock frequency is nearly five times faster. Speedup can be calculated as

Speedup= CTold / CTnew...(1)

Therefore, the latency of each instruction is ideally unmovable; however the throughput is ideally five times better. Overall CPU time for the processor can be calculated as

CPU Time= No. of Clock Cycles * Clock Cycle Time ...(2)

Steps to design Pipelined MIPS are as follows:

1. Instruction Fetch Unit-	IR: Memory [PC]; PC := PC+4
2. Instruction Decode Unit-	A := Reg [IR[25:21]], B := Reg [IR[20:16]] ALUout := PC+ Sign_extend[IR[15:0]]
3. Execute| Memory Address| Branch Unit-	Memory : ALUout := A+ IR[15:0] R-Type : ALUout := A op B Branch : if A=B then PC := ALUout

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4. Memory access| R-Type Unit- Lw : MDR := Memory[ALUout]
Sw : Memory[ALUout] := B
R-Type : Reg [IR[15:11]] := ALUout

5. Write Back Unit- Lw : Reg [[20:16]] := MDR

Instruction Fetch is the first stage in MIPS pipelined structure. Instruction code fetched from this stage which is obtained from the Instruction memory and then goes to next stage of pipeline. Instruction Decode is the second stage in this architecture. It has dual-port memory, Register file contains register data which read and write the register data according to the opcode operation, branch targets are also calculated in this stage. This stage is having control unit who decides what values must be set to, which depends upon the given instruction. Next stage is the execution unit having the executions performing in ALU block determined by ALUop signal coming from the previous stage. Branch address is calculated by adding the PC+4 to sign extend immediate field and shift left with 2 bits using adder. The next stage of pipeline is memory access, where Lw and Sw instructions access from the data memory block [8].

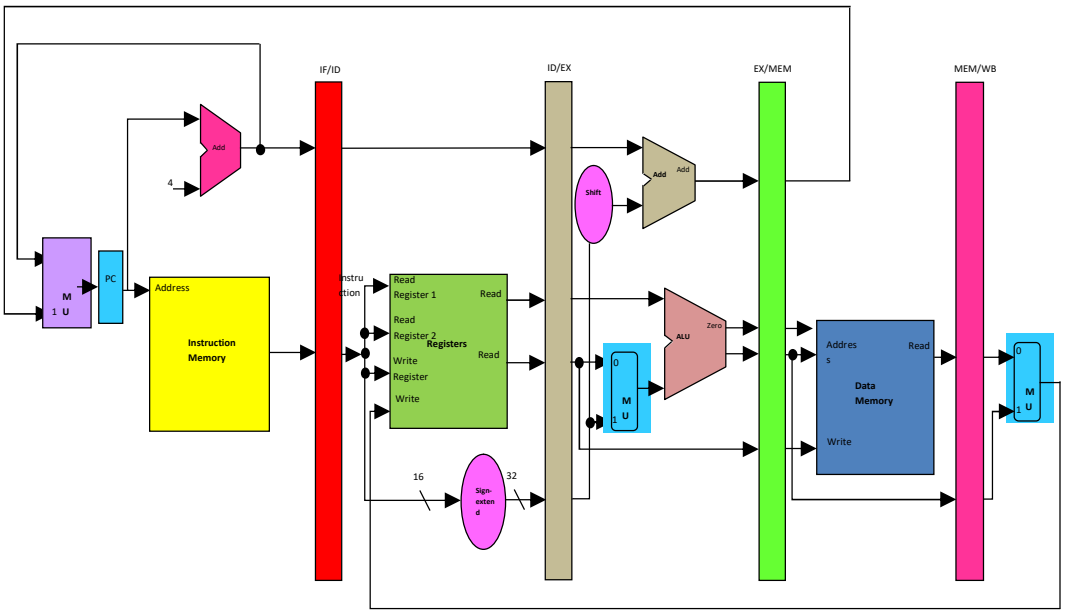

Fig.1. MIPS Datapath with five stage pipeline[8].

During the write-back stage, mutually instructions write back their results into the register file situated in the second stage of pipeline. This pipeline architecture has been shown in figure 1; Where the MIPS five stage pipelined datapath is containing all the architectural blocks. This datapath has control line which is controlling all the operations and instruction executions in the datapath.

POWER MITIGATION TECHNIQUES IN XILINX FPGAS

Power consumption of any electronic design can be divided into two principal categories that is, Static power and Dynamic power. Dynamic power in overall falls as transistors minimize, small transistors have low parasitic capacitances with shorter interconnects. By using different static and dynamic power reduction techniques, for instance, Triple Oxide Method, Transistor Distribution Optimization, Integrated Blocks, Clock Gating Enhancements, LUT4 vs LUT6 and I/O Power Reduction in Spartan-

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6. If we compare the two Spartan class FPGAs Spartan-6 with Spartan-3A, Then the result comes as, the normal static power in Spartan-6 devices is 50% lower and dynamic power is 40% lower. Xilinx has secured power reductions in Spartan-6 FPGAs by transforming on different levels of the FPGA design [18].

Low power methodology needs dynamic power reduction at all the design abstraction layers such as Architecture Level- Parallelism, Pipelining, Redundancy, Data Encoding; Circuit Logic Level- Energy Recovery, Logic Styles and Transistor Sizing; System Level- Partitioning and Power down; Algorithm Level- Complexity, Concurrency and Regularity; Technology Level- Threshold Reduction and Multi-threshold devices. Pipelining in DSP applications reduces the dynamic power by inserting the inputs regularly and decreases net-lengths and reduces glitches [21].

Static power is developed due to quiescent current inside the transistors composed of FPGA and switching of the transistors results in generation of dynamic power.

$$\mathbf{P\ (dynamic) = C.V^2.f} \quad \ldots(3)$$

$$\mathbf{f = Pdt.\ Fclk} \ldots(4)$$

Where, f= frequency at which the data transition happen and

Pdt= the probability of data transition

In HDL Modification Techniques, a well-organized and high quality HDL code can lowers the unwanted data toggling of design which results the ample amount of dynamic power saving. Likewise, logic optimization, removal of redundant logic and proper resource sharing in the RTL design helps to shrink on-chip power. The IOs power consumes maximum dynamic power. Power reduction can be attained at the IOs level [1]. Multiple Verilog HDL coding options are available to optimize the dynamic power for Xilinx FPGA such as: Synchronous reset design, Minimize local resets, Controlling the use of clock enables, Low power designing for Block RAM arrays, designing small memory buildings with LUTs(<4k bits)[20].

FUNCTIONAL SIMULATION AND RESULTS

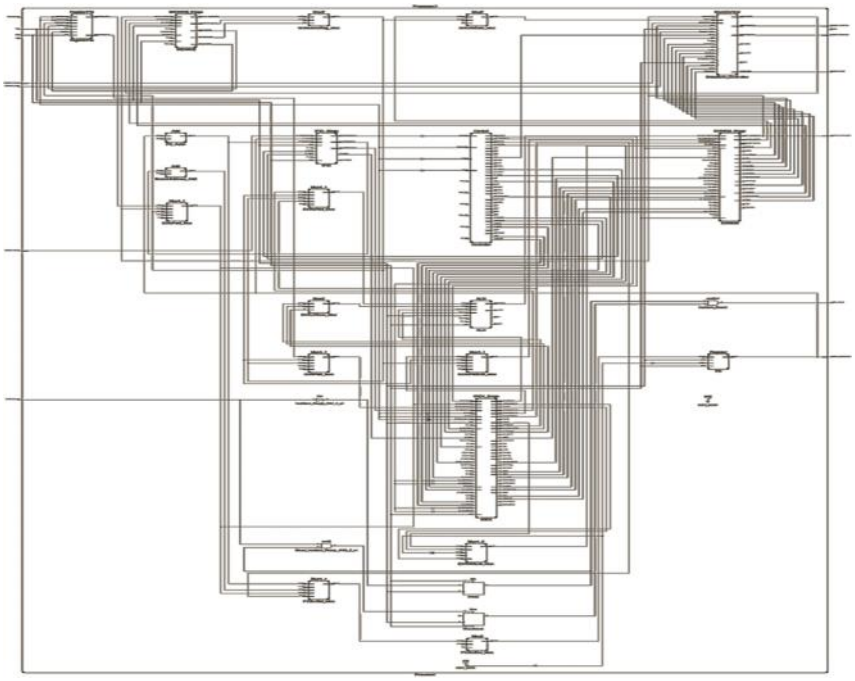

Fig.2. RTL Schematic for 32-bit RISC top entity

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The pin diagram of proposed five stage pipelined architecture of RISC containing RTL schematic view has been shown in Figure.2. Synthesized design has been created successfully on FPGA using Xilinx ISE 14.5. Figure.2. is the RTL (Register transfer level) representation of 32-bit RISC processor design. This representation (.ngr file created in XST) is generated using the Xilinx ISE. The intention of this level is to be as near as to the original HDL code. In the RTL design, the top entity is characterized in terms of blocks such as adders, multiplexers and look up tables. To check the module functionality of designed architecture with five stage pipeline, a set of instructions were executed perfectly on ModelSim 6.2c and simulation results are showing in Figure 3.

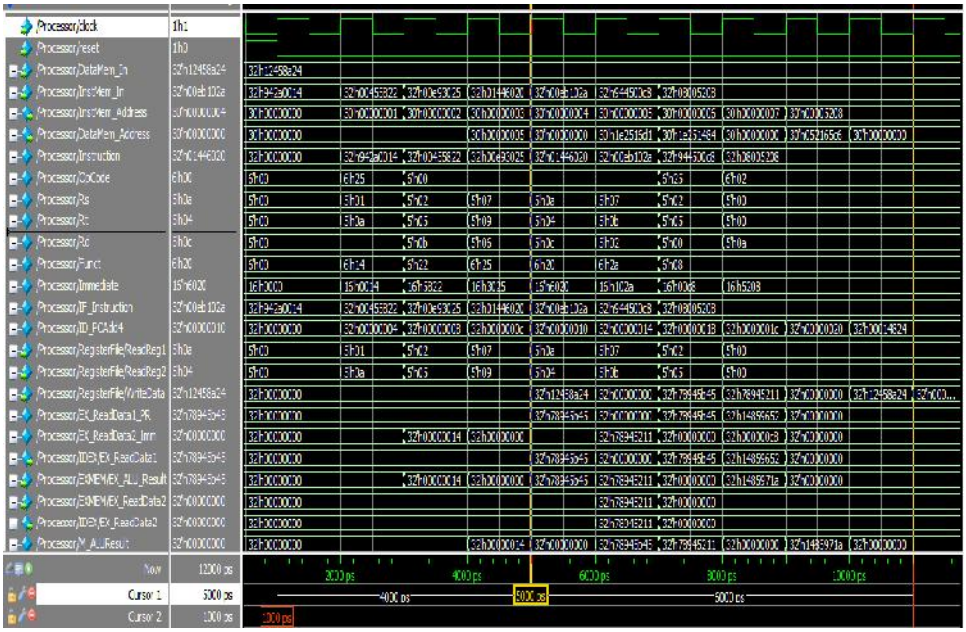

Fig.3. Simulated Results of 32-bit Pipelined CPU using ModelSim 6.2c

Table 1. Summary of Power Optimization On FPGAs

On Chip Power Consumption	Normal Power of RISC (mW)	Power Optimized using DLX architecture (%)	Power Optimized Designed using MIPS on SPARTAN- 3E (%)	Power Optimized Designed using MIPS on SPARTAN- 6 (%)
Clock	5.80	19.32	31.04	-1.55
Logic	3.39	2.07	8.56	-1.76
Signals	7.99	9.39	37.43	-1.12
IOs (dynamic power)	37.74	48.79	54.96	60.26
MULTs	0.82	0	0	0
Quiescent	99.28	0.32	0.59	19.42
Total	155.03	13.33	17.04% Vccin= 1.23V	22.72% Vccin= 1.23V

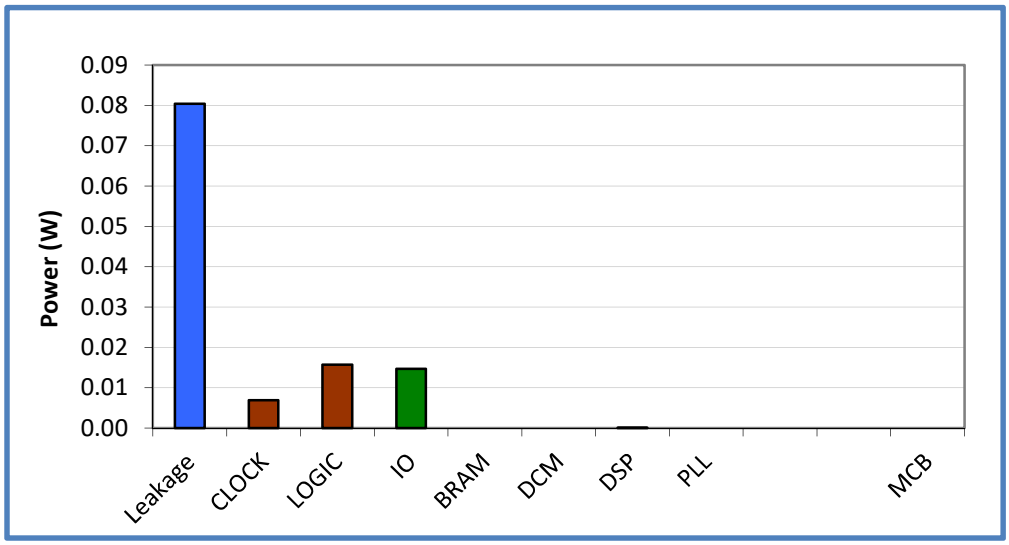

Fig.4. On-chip power by function (Vccint= 1.23V) for Spartan-6

The design was synthesized and analyzed for two different Xilinx Spartan class FPGAs. Spartan-3 and Spartan-6 (90nm and 45nm) FPGA chips operates at different operating frequencies and voltages. On-chip power consumption has been calculated using Xpower analyzer and estimated Xilinx power estimator tool, which gives accurate results as per the synthesis. To get the accurate results of total power consumption, .ncd, .xpa and physical constraint file (.pcf file) need to be loaded into XPA which is generated while implementation. Obtained power analysis and produced results have been mentioned in Table.1.

CONCLUSION AND FUTURE WORK

The high performance 5 stage pipelined MIPS- based 32-bit processor has been designed using Verilog HDL. Synthesis report for the target FPGA device shows that the proposed design has 5 levels of logic and delay of 14.202ns and maximum operating frequency of 70.413MHz for Spartan-6. Some blocks of the design have been implemented and are running successfully on the target device using bit file. Power consumption of pipelined RISC was 119.82mW and 128.62mW for Spartan-6 and Spartan-3, and the total reduced power achieved is 22.72% for Spartan-6 which gives better results on power optimization using HDL power reduction techniques.

The future scope of this work includes: We can increase the number of instructions and additional pipelined stages, which can improve the performance in the CPU design. And can enhance the total throughput of the design. Hazard detection and Interrupt facility can be added to get the increased speedup of processor. Mitigation of power can be performed at different layers as mentioned before. Power calculation and reduction can be possible for different FPGA Technologies.

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