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Design of Priority Based Optimized Reversible Comparator

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ABSTRACT: Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. This project presents a Design of Priority Based Optimized Reversible 4 bit Comparator using different single bit Reversible comparators and TR and BJN comparator. All the proposed comparators have been designed in VHDL and synthesised and simulated in ALTERA QUATRUS –II 9.1. From the results have shown that the proposed design used 5 Combinational ALUTs.

Keywords: CMOS, BJN comparator.

1.INTRODUCTION OF ONE-BIT IRREVERSIBLE COMPARATOR

The conventional one-bit irreversible numerical comparator, which consists of two NOT gates, two AND gates and one NOR gate [10], is shown in Fig.3a with its truth table in Table 1.1 We can get the following logic expressions from Table 1.1.

Table 1.1. Truth table of 1- bit comparator

Input		Output		
A	B	$F_{A>B}$	$F_{A<B}$	$F_{A=B}$
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

It is observed from the above table that, if any two conditions are not satisfied, it is understood that the third condition will be true. So one of the outputs can be generated from the remaining two outputs and thus the design can be optimized.

In the proposed one-bit comparator design, we have considered $F_{A>B}$ and $F_{A=B}$ and the third condition $F_{A<B}$ is generated from the first two outputs. Hence the design expression leads to

This design requires one NOT gate, one AND gate and one ENOR (Ex-Nor) gate and one NOR gate.

$$\begin{cases} F_{A>B} = A\overline{B} \\ F_{A=B} = \overline{A \oplus B} \\ F_{A<B} = \overline{(A \oplus B)} \cdot \overline{(A\overline{B})} \end{cases}$$

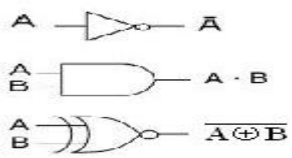

Fig 1.1 a. Irreversible gates for Numerical comparator

1.1THE EXISTED ONE BIT REVERSIBLE COMPARATOR DESIGNS

All the gates mentioned in section 2 can be used for the construction of reversible comparators. Here the proposed BJN gate is used in the last stage of comparator to generate all the outputs of comparator. Using this gate in combination with existing reversible gates, garbage output, quantum cost and gate counts are reduced.

1.1.2 One- bit comparator using Peres and BJN gate

Reversible one bit comparator is implemented with Feynman gate and Peres gate and BJN gate as shown in fig.1.2 The number of garbage outputs are

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two and represented as G1 and G2, it uses three constant inputs one logic ‘0’ and two logic ‘1’.

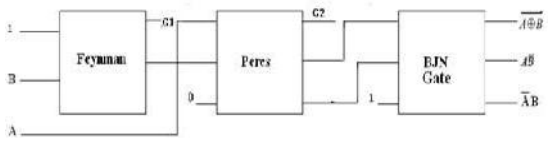

Fig.1.2one bit comparator using Peres gate

1.1.3 One bit comparator using Toffoli and BJN gate

Reversible one bit comparator is implemented with Feynman gate and Toffoli gate as shown in fig1.3 The number of garbage outputs are two and represented as G1 and G2, it uses three constant inputs , one logic ‘0’ and two logic ‘1’ it requires one Feynman gate and two Toffoli gates.

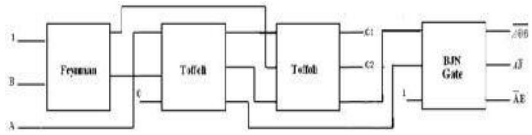

Fig. 1.3.one bit comparator using Toffoli gate

1.1.4 One bit comparator using R and BJN gate

Reversible one bit comparator is implemented with Feynman gate and R gate as shown in fig1.4 The number of garbage outputs is two and represented as G1, it uses two constant logic ‘1’ input. It requires one Feynman gate and one R gate.

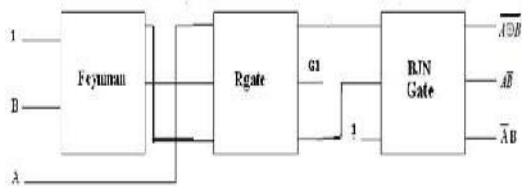

Fig 1.4 one bit comparator using R gate

1.1.5 One bit comparator using URG and BJN gate

Reversible one bit comparator is implemented with Feynman gate and URG gate as shown in fig 1.5 The number of garbage outputs are three and represented as G1,G2 and G3.It uses Four constant inputs two logic ‘0’ and two logic ‘1’. It requires one Feynman gate and two URG gates and one BJN gate

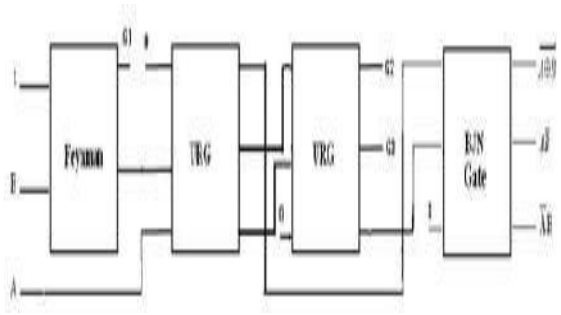

Fig.1.5 one bit comparator using URG gate

1.1.6 One bit comparator using Fredkin and BJN gate

Reversible one bit comparator is implemented with Feynman gate and Fredkin gate and BJN gate is as shown in fig.3.2e. The number of garbage outputs are six and represented with G1 to G6, it uses seven constant inputs, four logic ‘0’ and three logic ‘1’. Two Feynman gates are used for fan-out purpose in the input part.

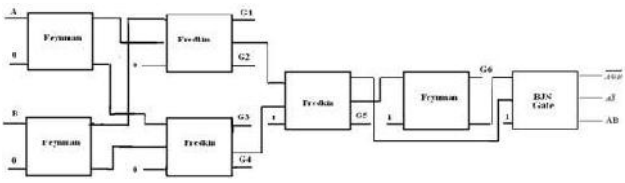

Fig1.6 one bit comparator using Fredkin gate

1.1.7one bit comparator using TR and BJN gate

Reversible one bit comparator is implemented with Feynman gate and TR gate and BJN gate as shown in fig.3.2f. The number of garbage outputs are two and represented with G1 and G2, it uses three constant inputs, one logic ‘0’ and two logic ‘1’.

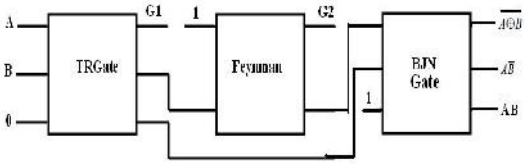

Fig1.7 one bit comparator using TR gate

2.THE PROPOSED FOUR BIT REVERSIBLE COMPARATOR DESIGNS

All the gates mentioned in section 1 can be used for the construction of reversible 4 BIT comparators. Here the proposed BJN gate is used in the last stage

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of comparator to generate all the outputs of comparator. Using this gate in combination with existing reversible gates, garbage output, quantum cost and gate counts are reduced. Reversible 4 bit comparator is implemented with Feynman gate and Peres gate and BJN gate as shown in fig.2.1

Reversible 4 bit comparator is implemented with Feynman gate and Toffoli gate as shown in fig.2.2 Reversible 4 bit comparator is implemented with Feynman gate and R gate as shown in fig.2.3 Reversible 4 bit comparator is implemented with Feynman gate and Fredkin gate and BJN gate is as shown in fig2.4. Reversible 4 bit comparator is implemented with Feynman gate and TR gate and BJN gate as shown in fig2.5.

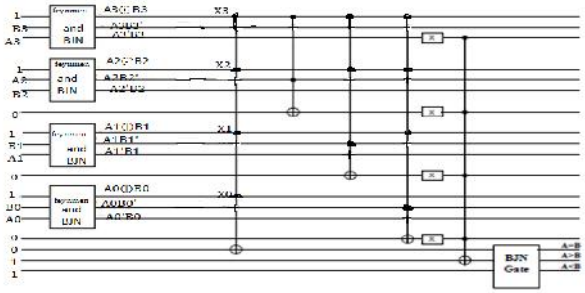

Fig 2.1: 4 BIT comparator using Feynman,Peres and BJN gate

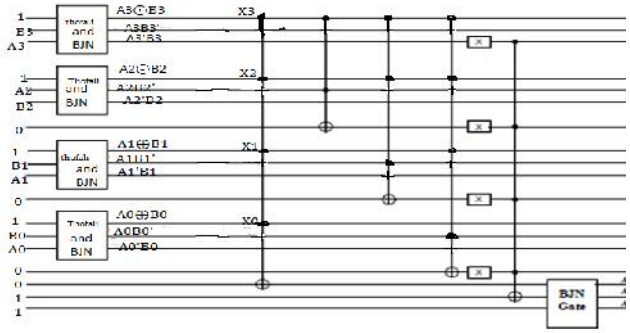

Fig2.2: 4 BIT comparator using Thofali and BJN gate

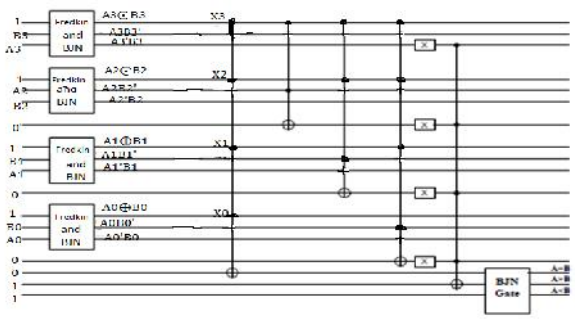

Fig 2.4: 4 BIT comparator using Fredkin and BJN gate

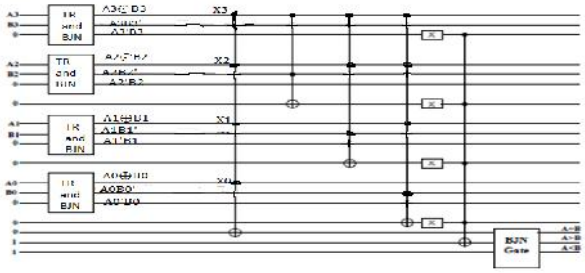

Fig 2.5: 4 BIT comparator using TR,Feynman and BJN gate

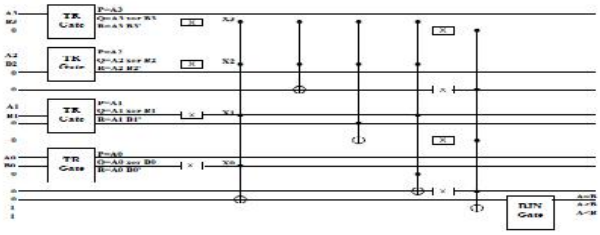

Fig 2.6: 4 BIT comparator using TR and BJN gate

Flow Status	Successful - Fri Apr 28 01:13:03 2017
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	comparator
Top-level Entity Name	comp4_ver1
Family	Stratix II
Device	EP2S15F672I4
Timing Models	Final
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	5 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	11 / 366 (3 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)

Fig 2.7: 4 bit comparator using TR and BJN gates Design summary.

The above figure is representation of design summary for four bit comparator using TR and BJN gates is implemented in one of the FPGA Family is QUARTUS II version and StratixII family. The above one bit comparator takes 5 combinational ALUTs and totally 11 Input and output pins.

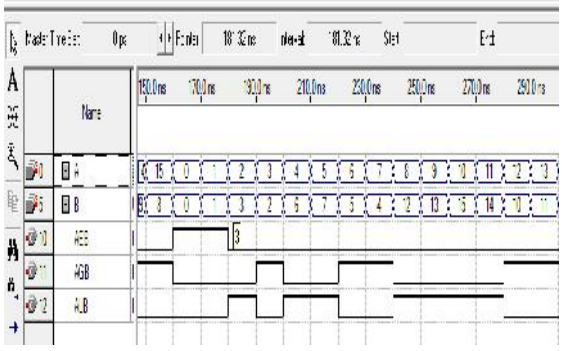

Fig 2.8: Simulation Results for 4 bit comparator using TR and BJN gates

Flow Status	Successful - Fri Apr 28 01:15:01 2017
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	comparator
Top-level Entity Name	comp4_ver2
Family	Stratix II
Device	EP2S15F672I4
Timing Models	Final
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	5 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	11 / 367 (3 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)

Fig 2.9: 4 bit comparator using TR and BJN gates Design summary

The above figure is representation of design summary for four bit comparator using any one of the abve one bit comparator and BJN gates is implemented in one of the FPGA Family is QUARTUS II version and StratixII family. The above one bit comparator takes 5 combinational ALUTs and totally 11 Input and output pins.

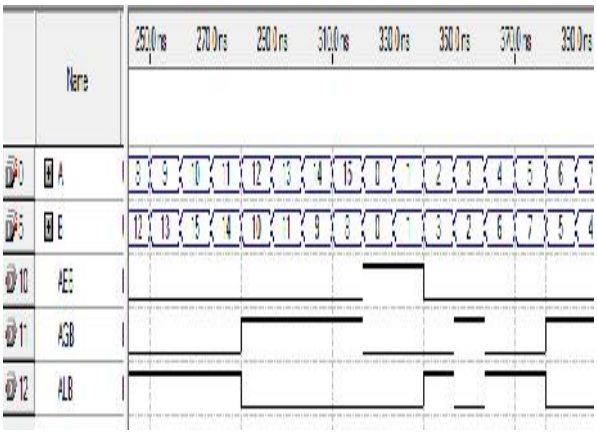

Fig 2.10: Simulation Results for foue bit comparator using TR and BJN gates

CONCLUSION

In this paper an optimized reversible comparator is presented with the proposed new Reversible BJN gate. The design is very useful for the future computing techniques like ultralow power digital circuits and quantum computers. It is shown that the proposal is highly optimized in terms of number of reversible logic gates, number of garbage outputs and number of constant inputs.

This paper presents a Design of Priority Based Optimized Reversible 4 bit Comparator using different single bit Reversible comparators and TR and BJN comparator. All the proposed comparators have been designed in VHDL and synthesised and simulated in ALTERA QUATRUS –II 9.1. From the results it is evident that the proposed design used 5 Combinational ALUTs and operating with 84.01MHz frequency.

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