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Comparative Analysis of Various Fast Adder Circuits in Different Deep Sub-micron Technologies

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Abstract—The adder is one of the most tedious circuits whichrequires considerable design effort in order to achieve high speed operations. Many adder designs show high performance by reducing the delay of the critical worst path, compromising other parameters like power dissipation thereby affecting power delay product.In this paper, 16 bit Carry Skip Adder and 16 bit Group Carry Look-ahead Adder are compared based on propagation delay, static and dynamic power dissipation in 300nm, 130nm and 90nm technologies. Circuit design and simulation have been performed in Electric Version 9.05 to come up with optimum wide adder.

Keywords: Group Propagate, Group Generate,Propagation Delay, Power Dissipation, Carry Lookahead, Carry Skip

1. Introduction

The adder is the logic circuit which is designed to execute fast arithmetic operations and find extensive use in other operations like subtraction, multiplication and division [1]. Basically use of adders is mainly done in the arithmetic logic in digital processors. These are also used in other areas to calculate addresses,table indices etc. The speed of adder plays a significant role in designing therefore to reduce propagation delay,extensive research has been going on . The speed limitation in design of adder circuit is the propagation of carry bits from one stage to another [2]. The 1 bit Full adder circuit is the basic building block in any adder circuit.A N-bit ripple carry adder circuit is made by cascading N number of full adders.This kind of network is called an repetitive logic device array . [3].The full adder is considered as a block and the ripple carry adder is considered to be an array.Due to the rippling of carry from one block to other block,the delay increases considerably for n bit adder as n advances.So many high speed adders such as carry select logic adder , carry save logic adder, carry skip logic adder etc. have been recommended to reduce the propagation delay of the output carry bit .In this paper to improve the speed of adder the Carry look ahead concept is proposed.This avoids the rippling of carry by introducing group or block propagate and group or block generate.The block propagate and block generate calculate the carry in advance which increases the speed of adder. Section 2 describes the optimum way for carry propagation with details of ripple carry adder, carry skip logic adder and carry lookahead logic adder. Section 3 provides design of wide adders for different sub-micron technologies. Sim-ulation results have been shown in this section along with comparison of propagation delay and power dissipation for different adder designs. Section 4 concludes this paper and section 5 enlightens about future scope in this area.

2. Carry Propagation Optimization

Speed of adder is mainly limited by time taken to propa-gate the carry from 1 block to another in case of wide adders. This section throws light on different adder designs and suggests optimized design for reduced propagation delay in sub-micron technology.

2.1. Ripple Carry Adder (RCA)

Ripple carry adder executes the addition of two n-bit numbers and it produces n bit output sum or addition and carry output bit.The ripple carry adder is designed by interconnecting n number of 1 bit full adders.The carry bit generated as the output from previous adder is fed to the input carry of next full adder circuit.Figure 1 [11]shows the array of four full adder (FA) circuits to generate the circuit of 4 bit adder with rippling effect.The Least significant bits

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$a_0$and $b_0$are added to generate the sum $s_0$and carry c_1.The output bits generated from each adder are considered as output sum bits depicted as s_0-s_3. The final output sum

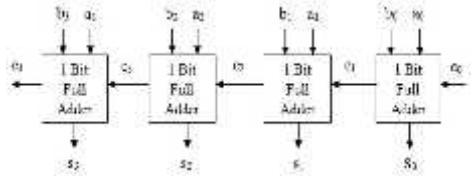

Figure 1. 4 bit Ripple Carry Adder

and final output carry of ripple carry adder depend on the carry generated by previous block.The higher order bit i.e. $s_3$is obtained only after rippling of the carry signal fromsuccessive stages.Therefore the sum and carry bits are valid after a significant delay.In design of n-bit adder the critical path delay is 2n+ 2 gate delays.Thus, for a 16-bit adder, the longest path delay is 34 gate delays [4]. As 'n' increases, this design becomes obsolete because of longer and longer rippling delays.

2.2. Carry Skip Adder

The carry-skip circuit is also referred as carry bypass logic.It shows an improvement over RCA having a carry bypass path [5]. The improvisation of worst-case delay is done by using connection of carry-skip adders to form a block-carry-skip adder. When each adder block has a group propagate signal equal to 1, significance of it is that it will show propagate signal of each stage high and the same carry will propagate through all stages showing delay in generation of final carry bit .In above case the circuit passes the same carry bit as the input to the next stage skipping intermediate adder block [6]. The carry skip circuit comprises of the AND gate which accepts the input carry bit of the same stage and compares it to the group propagate signal using the propagate values of each stage . The OR gate present in carry skip circuit performs operation on two bits ,one bit from the output of the AND gate and the other bit is c_{j+4} ,the output carry generated from the same stage.The output of carry skip circuit given in equation 1 is passed as input carry bit to the next stage.

$$carry = c_{j+4} + p_{[j,j+3]}.c_j \qquad (1)$$

If $p_{[j,j+3]} = 0$, then c_{j+4} decides the carry-out of the group. Also for next condition if $p_{[j,j+3]} = 1$ and carry-in bit c_j= 1, then the group carry-in is directly sent to the nextgroup of adders without delay. If the condition $p_{[j,j+3]}.c_j$ is true, then the carry-in bit skips the entire block [11].The value of j ranges from adder produces a carry out bit of c_1 = 1. The size of a carry-skip block affects the overall speed of the scheme. Variable k-value can also be used for better performance.

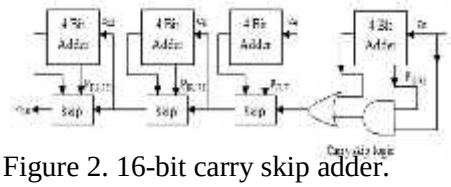

Figure 2. 16-bit carry skip adder.

0,1...n-1. 16 bit carry skip adder is shown in Figure 2. The size of the carry-skip group has been chosen as k=4 for every segment. The worst-case delay through this circuit is when c_0 = 0 and the 0^{th} bit

2.3. Carry Lookahead Adder (CLA)

Weinberg and Smith in 1956 [7] implemented CLA adder and it decreases carry propagation delay even after in-crease in number of inputs.But circuit complexity increases as number of inputs increases.Carry look ahead circuits are analysed for designing of high performance digital circuits, where speed of the processor is of important concern and these circuits are used as their propagation delay time ex-hibits logarithmic relation with the size of adder [8].CLA circuits are proved as one of the best circuit topologies in performance amongst wide adders. These circuits resolve delay problem of carry bit by calculating the carry signals of all stages in advance from input bits . It is based on the fact that a carry signal will be generated in two cases [11]:

(1) when both bits aj and bj are 1,where j represents bit value from 0-3 in 4 bit adder.

or (2) when one of the two bits is 1 and the input carry is 1.

$$c_{(j+1)} = a_j.b_j + (a_j \bigoplus b_j).c_j \qquad (2)$$

$$s_j = (a_j \bigoplus b_j) \bigoplus c_j \qquad (3)$$

The above two equations are represented in terms of two new signals P_j and G_j as shown in Figure 3 [11]:

$$c_{(j+1)} = G_j + P_j.c_j \qquad (4)$$

$$s_j = P_j \bigoplus c_j \qquad (5)$$

Where,

$$G_j = a_j.b_j \qquad (6)$$

$$P_j = a_j \bigoplus b_j \qquad (7)$$

The G_j and P_j are called the carry generate and carry propagate terms,for example carry generate at second stage will be G_2. The generate signal and propagate signals are obtained only from the input signal bits for addition and

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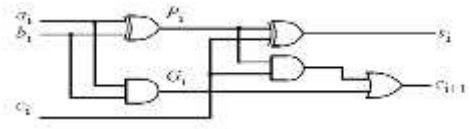

Figure 3. Generation of Pj and Gj Signals.

thus will be available within one or two gate delays. As the equation 4 is used to derive carry signal output at each stage , it has been observed that the output carry bit is not necessarily dependent on previous output carry signals [11]. Applying this to a 4-bit adder and putting j=0, 1, 2, 3 ..n-1 in equation 4, we get equation

$$c_1 = G_0 + P_0 .c_0 \quad (8)$$

$$c_2 = G_1 + P_1.G_0 + P_1.P_0.c_0 \quad (9)$$

$$c_3 = G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.c_0 \quad (10)$$

$$c_4 = G_3+P_3.G_2+P_3.P_2.G_1+P_3.P_2.P_1.G_0+P_3.P_2.P_1.P_0.c_0$$

(11) The carry-out bit c_{j+1}, of the final stage is obtained after four delays which consist of two gate delays to calculate the propagate term and to implement equation 8 [11]remaining two delays are required.A 4-bit CLA can now be built using the Pj and Gj signals and a logic block to generate the carry out signals according to equations 8-11. By using carry look-ahead technique, the time required for carry signal to propagate is reduced to four gate levels.

to propagate is reduced to four-gate level . Generationof the carry using above equations becomes tedious if wego for wide adders. This can be avoided by using 4-bit CLA blocks in hierarchy to realize adders with multiples of 4 bits. The simple basic implementation of 16-bit carry lookahead adder is shown in Figure 4. Cascading of blocks in such a way that carry out of present block acts as carry in for next block results in a ripple effect [10].Each block follows carry lookahead mechanism, thus addition operation of all blocks commence in parallel but each block has to wait until the carry out bit of previous block starts the operation hence introducing considerable delay. An improvement over this design is a 16-bit Group

Figure 4. 16 bit Ripple Carry Lookahead Adder.

Carry Lookahead Adder (Figure 5 [11]) consisting of four 4-bit CLAs, with additional group carry lookahead logic. As shown in figure, 4 CLAs are in cascaded form which generates group propagate and group generate signals.These output signals are fed as inputs to the next level CLA which generates a group propagate and group generate signal as output.In this logic,Group Generate (GroupG) and Group Propagate (GroupP) signals are accepted as input and carries in between the blocks are generated. Each CLA has a longest path with 5 gate delays. In the Group Carry Lookahead Logic section, Group Generate (GroupG) and Group Propagate (GroupP) signals are generated with 3 gate delays; carry signals are generated in 2 more gate delays, resulting in 5 gate delays to generate the carry out of each GCLA group and 10 gates delays on the worst case path (which is s_{15}-not c_{16}). Thus, this design can be more efficient than many other adder circuits.The Group generate signal output from this GCLA block is nothing but the final carry c_{16} signal.

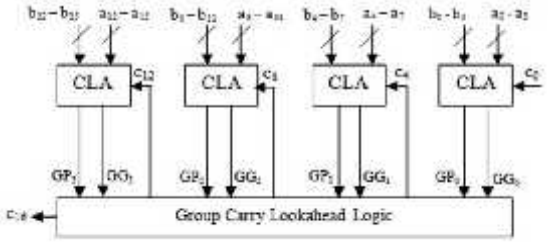

Figure 5. 16 bit Group Carry Lookahead Adder.

$$GroupG_0 = G_3 + P_3.G_2 + P_3.P_2G_1+P_3.P_2.P_1G_0 \quad (12)$$

$$GroupP_0 = P_3.P_2.P_1.P_0 \quad (13)$$

$$c_4 = GroupG_0 + GroupP_0.c_0 \quad (14)$$

$$c_8 = GroupG_1 + GroupP_1.c_4 = GroupG_1 + GroupP_1.GroupG_0 + GroupP_1.GroupP_0.c_0 \quad (15)$$

$$c_{12} = GroupG_2+GroupP_2.c_8 = GroupG_2+GroupP_2.GroupG_1+GroupP_2.GroupP_1.GroupG_0+GroupP_2.GroupP_1.GroupP_0.c_0 \quad (16)$$

$$c_{16} = GroupG_3+GroupP_3.c_12 = GroupG_3+GroupP_3.GroupG_2+GroupP_3.GroupP_2.GroupG_1+GroupP_3.GroupP_2.GroupP_1.GroupG_0 +GroupP_3.GroupP_2.GroupP_1.GroupP_0.c_0 \quad (17)$$

3. Results

In this paper, 16-bit Carry Skip and Carry Lookahead Adder circuits have been implemented in Electric software. These adder circuits have been compared for Static and Dynamic Power Dissipation, Propagation Delay in 300 nm, 130 nm and 90 nm technologies.

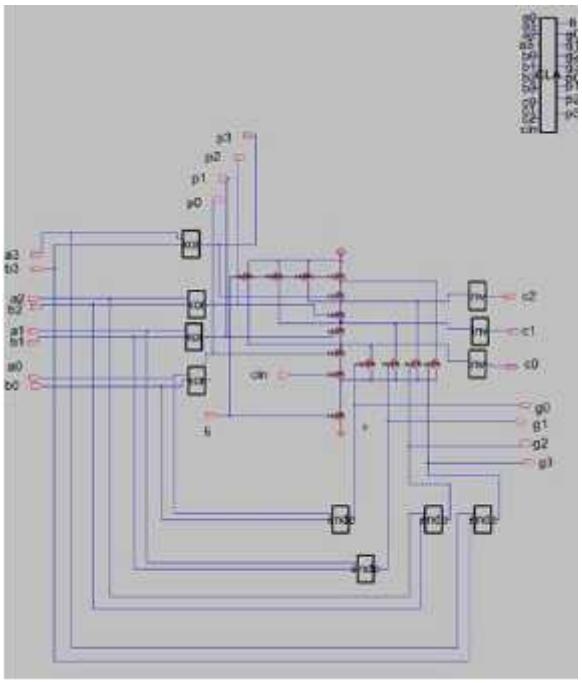

Figure 6. 4-bit MODL Adder

3.1. Implementation of Adder Circuits

16-bit Carry Skip and Carry lookahead Adders have been implemented in Electric V9.05 software. 4-bit Adder circuit using MODL,Multiple Output Domino Logic) is shown in Figure 6.

3.1.1. 16-bit Carry Skip Adder.

Figure 7 shows Carry Skip Adder Circuit for 16-bit addition implemented using MODL. W/L ratio of PMOS to NMOS transistor has been chosen to be 2:1.

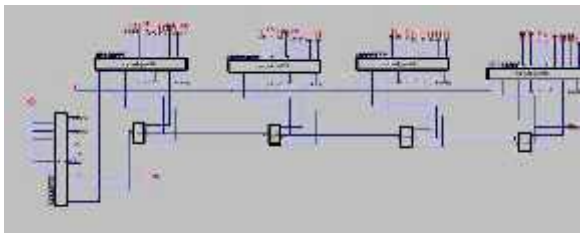

Figure 7. 16-bit Carry Skip Adder Circuit

3.1.2. 16-bit Carry Lookahead Adder.

Group Generate and Group Propagate Signal Generation has been included in Figure 8 and Figure 9 shows 16-bit Carry Lookahead Adder Circuit implemented using Group Generate and Propagate Signals and thus avoiding rippling of carry from one block to another.

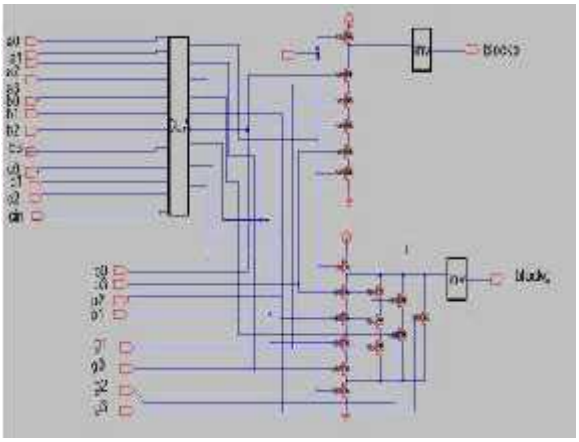

Figure 8. Group Generate and Propagate Signal Generation

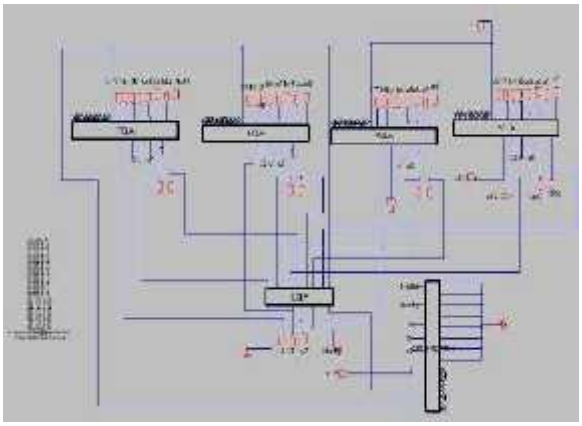

Figure 9. Carry Lookahead Circuit

3.2. Result Analysis of Adder Circuits

Figure 10 shows the output carry signal and power dissipation of 16-bit carry skip adder in different deep submicron technologies.

Figures 11 and 12 depict comparative analysis of carry skip and carry lookahead adder in terms of power dissipation and propagation delay respectively in different technologies. Results show that Carry Lookahead Adder performs better in terms of propagation delay as compared to Carry Skip Adder in 300 nm technology and as technology improves, performance of both the adders has been found to be comparable.As technology improves from 300nm to 90 nm static and dynamic power dissipation reduces,thus making circuit more efficient in term of power.

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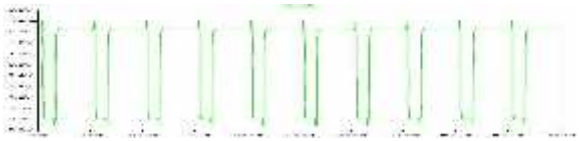
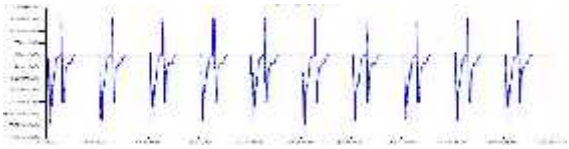
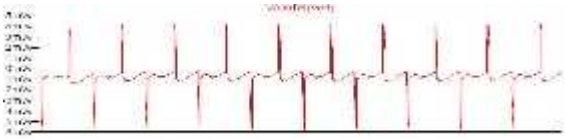
Final Carry Out of Carry Skip Adder



Power Dissipation in 300nm Technology



Power Dissipation in 130nm Technology



Power Dissipation in 90nm Technology technologies

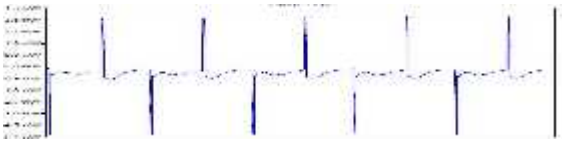


Figure 10. Carry output and Power Dissipation in different technologies for Carry Skip Adder

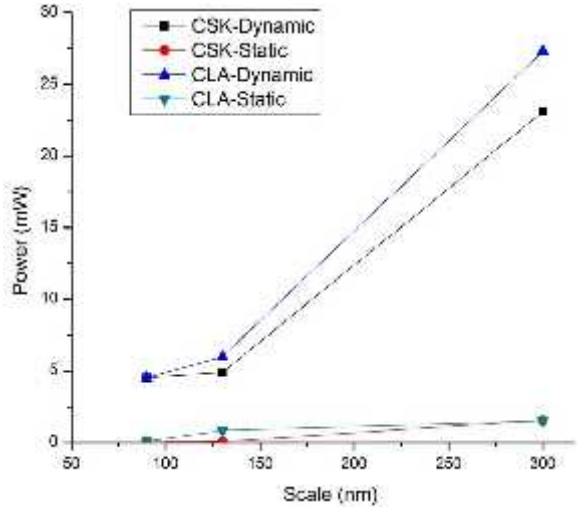


Figure 11. Power dissipation in different sub-micron technologies

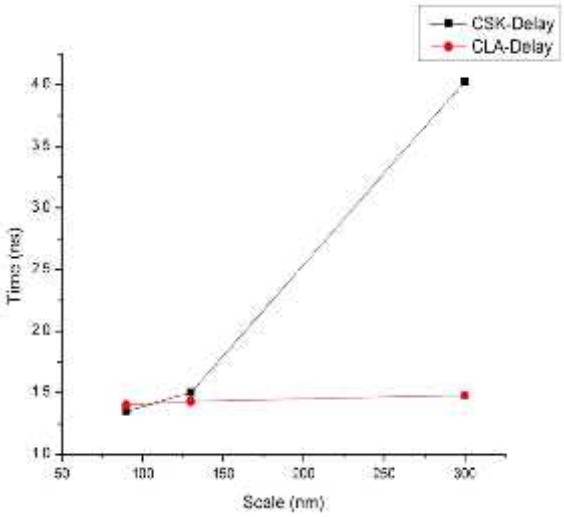


Figure 12. Propagation delay in different sub-micron technologies

4. Conclusion

In comparison with ripple Carry Adder, the propagation delay of Carry Lookahead Adder and Carry Skip Adder have been improved due to reduced rippling effect. In CLA, rip-pling of carry is avoided by using concept of group generate and group propagate signals and hence it has been found that this circuit has less propagation delay than Carry Skip Adder in 300 nm technology. As we proceed towards deep sub-micron technology, improvement has been observed in prop-agation delay and power dissipation. Comparative results have also shown that, in 130 nm, 90 nm technologies, Carry Skip and Carry Lookahead Adders have comparable values of propagation delay and power dissipation. Hence power delay product improves in deep sub-micron technology.

5. Future Scope

The results have been compared after simulation of

16 bit adder using carry skip and carry lookahead concepts. The same can be expanded up to 64 and 128 bit adder.

The results can also be seen by using technology beyond 90 nm.

The results can be compared with other type of fast adder circuits like carry select, carry save adders. Variable k skip adder circuit can be implemented for better performance.

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