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High Performance of Booth Multiplier For DSP

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ABSTRACT

A high speed complex multiplier design using Vedic Mathematics to improve the performance of the DSP applications.

Vedic Mathematics is the ancient methodology of Indian mathematics which has a unique technique of calculations based on 16 Sutras (Formulae). A high speed complex multiplier design (ASIC) using Vedic Mathematics is presented in this paper. The idea for designing the multiplier and adder, subtractor unit is adopted from ancient Indian mathematics "Vedas". On account of those formulas, the partial products and sums are generated in one step which reduces the carry propagation from LSB to MSB.

This paper proposes the hardware implementation of VLSI architecture for High Speed VLSI Design of Complex Multiplier Using Vedic Mathematics that have been modified to improve performance. This project was implemented in Verilog the coding is done in Verilog HDL and the FPGA synthesis is done using Xilinx Spartan library.

1. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications other element with absolutely different properties. These polymers can be made into granules, powders and liquids and that becoming raw resources for plastic products.

Plastics products are necessary part in today's world. Due to their light weight, durability, energy efficiency, coupled with a faster rate of manufacturing the plastic products. Plastics are produced from petroleum derivates and they composed of hydrocarbons but also contain additives such as antioxidants, colorants and other stabilizers. Disposal of plastics wastes posses a great hazard to the environment and effective method has not yet been implemented. Plastics are non-biodegradable polymers mostly containing carbon, hydrogen, and few other elements like nitrogen by non-biodegradable in nature, the plastic waste major contributes are municipal non organic solid waste and waste-plastic should be recycled or scientific method of municipal solid wastes disposal. According to survey conducted on the year 12000 approximately 6000 tonnes of plastic wastes were generated per day in India, and in that only 60% of it was recycled, the remaining of 40% plastic wastes remains in cities. Today about 130 Million tonnes of plastics wastes produced per year all over the world, out of which 75 Million tonnes of wastes produced from petroleum.

1.1. Multiplication process

This algorithm uses addition and shift left operations to calculate the product of two numbers. Based upon the above procedure, we can deduce an algorithm for any kind of multiplication which is shown in figure

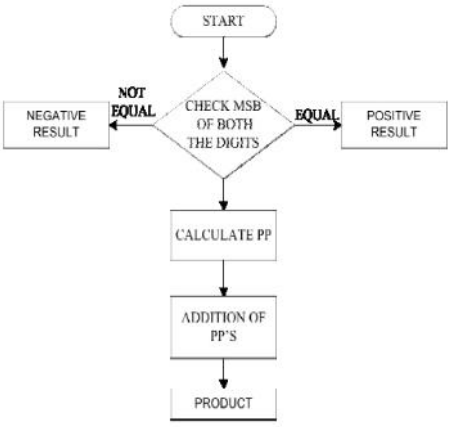

Fig.1.1. Multiplication process

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Fig.1.1 In the binary number system the digits, called bits, are limited to the set [0, 1]. The result of multiplying any binary number by a single binary bit is either 0, or the original number. Summing these partial-products is the time consuming task for binary multipliers. One logical approach is to form the partial-products one at a time and sum them as they are generated. Often implemented by software on processors that do not have a hardware multiplier, this technique works fine, but is slow because at least one machine cycle is required to sum each additional partial-product the reactor temperature the plastic starts to evaporate and these vapors leaving the reactor and passed into a condenser, (maintained at atmospheric temperature). The cyclone separator is provided at the end of condenser to separate the gaseous fuel and plastic liquid fuel compounds. The gas is reused to heat the pyrolysis unit and another end of cyclone separator is connected to a beaker in which the liquid hydrocarbon product (plastic oil) was collected. Temperatures and pressure were monitored continuously by using thermocouples and pressure gauge connected to it.

It is observed that in absence of catalyst, process gives about 60-62% yield, with 5 % natural zeolite yield is 65-67 % and with 5 % alumina catalyst it is about 70-71 %. An increase in the yield percentage and calorific value is observed with both the catalysts but higher effect is seen in case of oil obtained with alumina.

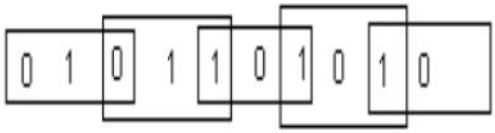

Fig.1.2. Grouping of bits from the multiplier term

Block	Re - coded digit	Operation on X
000	0	0 X
001	+1	+1 X
010	+1	+1 X
011	+2	+2 X
100	-2	-2 X
101	-1	-1 X
110	-1	-1 X
111	0	0 X

Table-1.1: Encoded data & multiplication operation on X

For the partial product generation, we adopt Radix-4 Modified Booth algorithm to reduce the number of partial products for roughly one half. For multiplication of 2's complement numbers, the two-bit encoding using this algorithm scans a triplet of bits. When the multiplier B is divided into groups of two bits, the algorithm is applied to this group of divided bits. Figure 4, shows a computing example of Booth multiplying two numbers "2AC9" and "006A". The shadow denotes that the numbers in this part of Booth multiplication

2 VEDIC MULTIPLICATION

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on some algorithms, some are discussed below:

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Triyakbhyam explained The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers.

2.1. Multiplication of two decimal numbers-

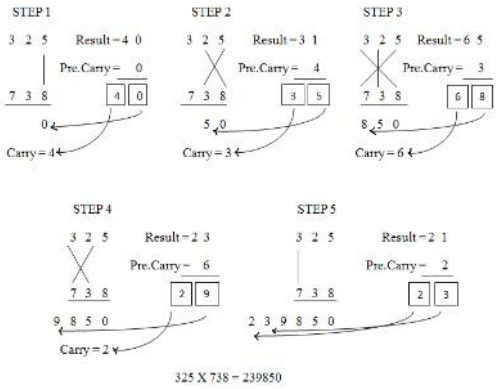

Fig 2.1 Urdhva Tiryakbhyam sutra

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Fig. 2.1 Each Multiplication operation is an embedded parallel 4x4 Multiply module.

To illustrate the multiplication algorithm, let us consider the multiplication of two binary numbers a3a2a1a0 and b3b2b1b0. As the result of this multiplication would be more than 4 bits, we express it as. r3r2r1r0. Line diagram for multiplication of two 4-bit numbers is shown in Fig. 2.2 which is nothing but the mapping of the Fig.2.1 in binary system. For the simplicity, each bit is represented by a circle. Least significant bit r0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier

3 Line diagram for multiplication

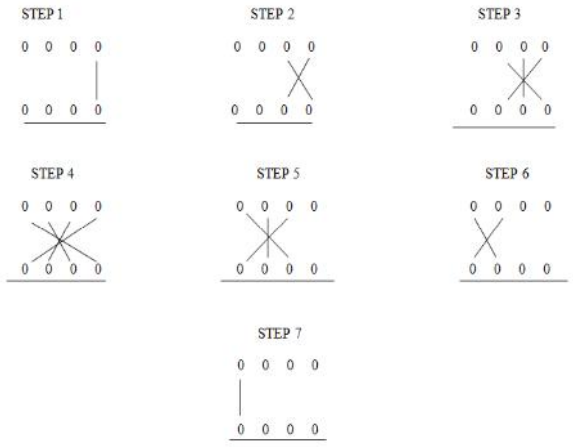

Fig 3.1 Line diagram for multiplication of two 4 - bit numbers

Fig 3.1 Firstly, least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position

Fig 3.1.1 Nikhilam Sutra

Nikhilam Sutra literally means “all from 9 and last from 10”. Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large.

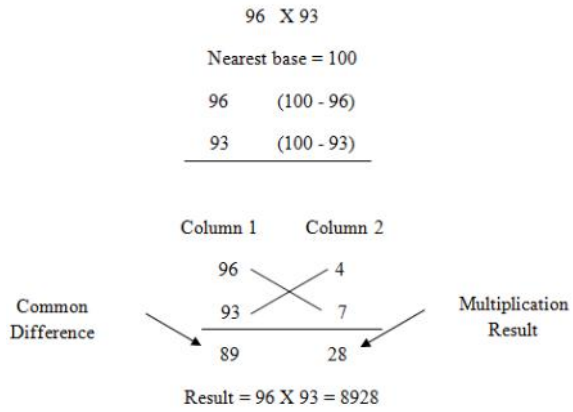

Fig 3.2 The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (7*4 = 28). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 96 - 7 = 89 or 93 - 4 = 89. The final result is obtained by concatenating RHS and LHS (Answer = 8928) [4].

Fig 3.1.2 Urdhva Tiryakbhyam sutra

Urdhva-Tiryak sutra

This is a general method applicable to any kind of multiplication. In this method starting from first digit on left, we go on multiplying crossways all digits and add them to get individual digits of the answer.

Each position is allowed only one digit, so digits in excess of one ar carried over to next multiplication-addition on the left side.

4SIMULATION AND SYNTHESIS REPORT

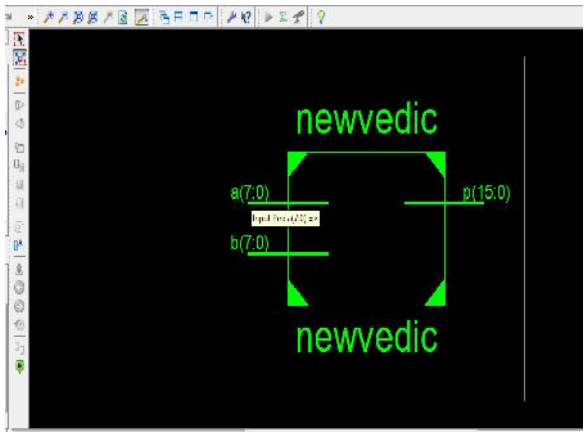

Fig 4.1 RTL Schematic Diagram Of Vedic Multiplier

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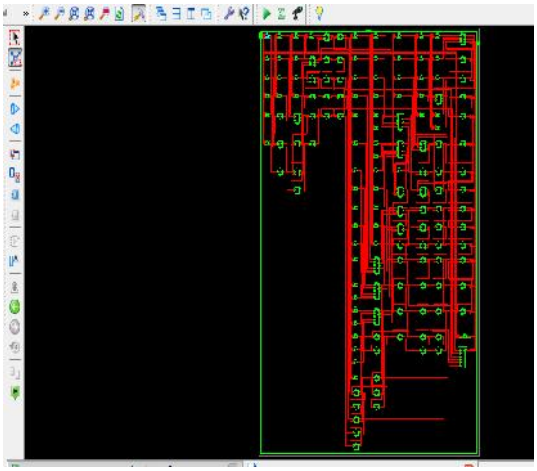

Fig 4.2 RTL Internal Schematic Diagram Of Vedic Multiplier

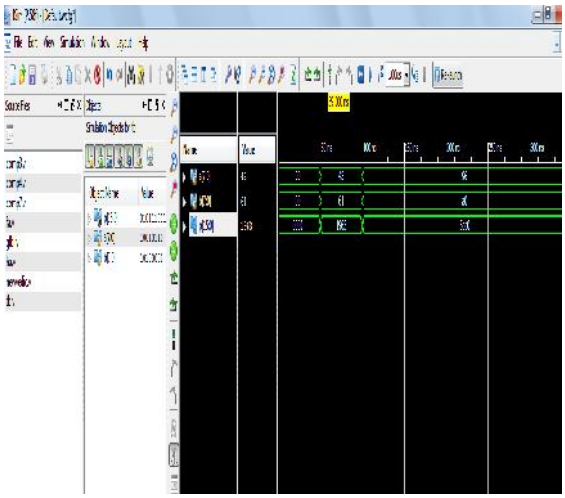

Fig 4.3 RTL Simulation Result Of Vedic Multiplier

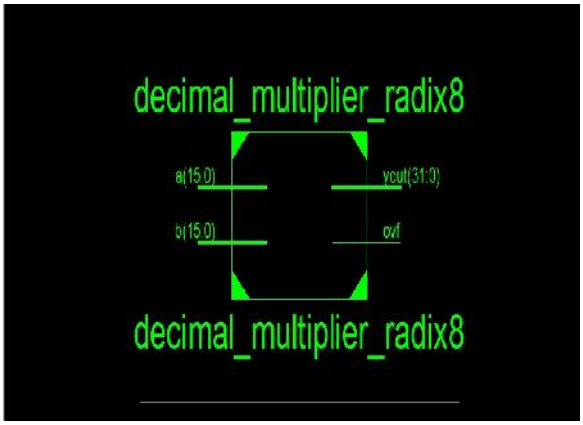

Fig 4.4 RTL Schematic Diagram Of Decimal Multiplier

Fig 4.5 Simulation result of Decimal Multiplier

5. CONCLUSIONS

From the tests conducted with waste plastic oil and diesel blends, the following conclusions are arrived

1. The proposed Radix-8 Multiplier may be used in DSP applications because it gives better performance in terms of power, delay and PDP.
2. The proposed adder based multiplier can be used in high speed application because of its less power dissipation and delay. Also, this multiplier has the minimum number of nonzero partial products based on the CSD numberproperty. an increase in brake power for all fuel and engine conditions.
3. The number of add/subtract operations is further reduced through the use of bypass techniques. Thus, the complexity of the hardware implementation is dramatically reduced as compared to conventional methods, including modified Booth recoding and competing CSD recoding techniques.

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