International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 9
September 2017

Academic Science

A Secure Mean for PC to PC Wireless Communication

Ms. Pranita Kanadkhedkar,
Assistant Professor,
MGM's College of Engineering, Nanded, MH, India.

ABSTRACT :

The main objective of this paper is to discuss a secure mean of Wireless Communication between two PCs. In hospitals, banks, colleges or in offices data can be safely and immediately transferred from one PC to another without requiring LAN or Cables etc. Text or data transfer between two PCs is achieved with this system over a distance of 50 ft. However there is a scope of increasing this distance further if speed and cost are not the constraints. Keeping in view, the advantage of very low noise FM transmitter is used for transmission of text. Then data is FSK modulated. The Mark and space frequencies are suitably frequency modulated by FM transmitter working at 90 MHz with transmitted power of 900 mW. The FM receiver and FSK demodulator are used to receive the original data. Data is serially transmitted. The system is half duplex asynchronous data system. However, by making little modifications in hardware full duplex system mode can also be achieved. This system is quite useful for data communication in industry, offices and specially in military work where security is a major concern. The results of the proposed device have been duly achieved by the author of the paper.

INTRODUCTION :

There are situations in which not just one computer is sµFficient to handle all works or different users require different computers for different works but the whole system should be communicated with each other to transform or receive information. Thus a media is required for information to be sent or received. Basically there are two types to achieve thisn : wired and wireless. Wired techniques involves LAN (Local Area Network), Ethernet, fiber optic etc. Wired networks are more secure, more reliable and offer a higher data speed. Wireless networks are more convenient when mobility is required and are sometimes the feasible choice (e.g. in old buildings where installing cable is difficult or impossible.) However, wireless networks can also pose a significant security risk when not properly installed or maintained. The Location and intended use must be considered while deciding between both. Here PCs are not using internet. With this system wireless communication between two PCs with lowered security risks is achieved. Here transmission of written text or file from one PC to another is done serially and asynchronously. By taking all benefits of FM transmission specially like high speed of transmission and low noise hardware part is designed. In hardware PS-282 to TTL converter i.e. IC 1489, FSK modulator (designed with IC XR 2206) and FM transmitter and transmitting antenna are main parts on transmission side. IC 1488 is TTL to RS-232 converter IC, FSK demodulator(ICXR2211) and FM receiver (designed with IC CXA 1619BS) and receiving antenna are the main parts on receiving side. Band rate for the data or file transfer achieved is 1 KBPS. For successful transmission of signal bandwidth required is 20-25 kHz.

The range covered between two PCs is 50 feet so it is very beneficial for transferring data in building premises without having any cabling between the PCs. Hence, the cost and maintenance of cabling is also saved in this way. Above this, if there is no constraints of speed and cost, communication area can still be increased further. Since the device consumes little hardware along with some software to transfer data or file from one PC to another, all worries related to internet i.e. server down or speed and security constraints are not applicable here.

Here, instead of using FSK modulator with FM transmitter other modulation techniques such as AM, PSK, QPSK or WLAN etc. can also be used. But under normal working conditions at mandate. Signaling speed, FSK may be employed with performance better than any other method under noisy environment. Again one of the important

reason behind the usage of FSK is that a constant modulated signal envelope is achieved. A little bit extra hardware is required for FSK receiver but many advantages such as equal digit error probabilities and fixed threshold level etc. overcome this drawback. Very high speed communication with no time delay is achieved with the help of this system.

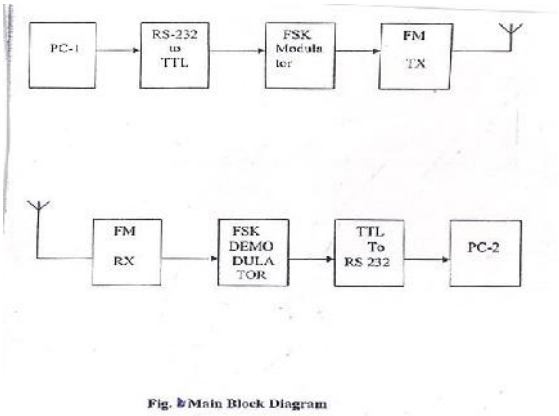


Fig. 1 Main Block Diagram

Circuit Design and Description :

Transmission section :

1) PC 1 & PC II :

There are two PC 1 and PC II, are used for display of transmitted & received text respectively.

2)RS 232 to TTL Conversion :

Here IC 1489 is used which do the conversion directly. It has very low power consumption and external filtering is also not required. When a character is written at transmitter side PC then it converted into its ASCH code and output voltage level is at either + 12 V or – 12 V, If it is + 12V then at the output of IC 1489 we get logic '0' and if it is – 12 V then it converted to logic '1'.

3)FSK Modulator :

Output of IC 1489 is given as FSK input. Here as FSK modulator IC XR2206 is a 16 pin monolithic function generator IC capable of producing high quality sine, square triangle, ramp and pulse waveforms of high stability and accuracy. The output waveform can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz. It has a typical drift specification of 20 ppm/degree C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage while maintaining low distortion and excellent stability. It has TTL compatible FSK controls.

The XR2206 is comprised of four functional blocks, a voltage controlled oscillator (VCO), an analog multiplier and sine shaper, a unity gain buffer amplifier and a set of current switches. The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to the ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using FSK input control pin. This input controls the current switches which selects one of the timing resistor currents, and routs it to the VCO.

The XR2206 can be operated with two separate timing resistors R_1 and R_2, connected to the timing pins 7 and 8 respectively. Depending on the polarity of the logic signal at pin 9 either one or the other of these timing resistors is activated. If pin 9 is open circuited or connected to bias voltage > 2 V only R_1 is activated. Similarly if the voltage level at the pin 9 < 1 V only R_2 is activated. Thus the output frequency can be keyed between two levels f_1 and f_2

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

Fig.2 shows the circuit connections for sinusoidal FSK signal operation. Mark and Space frequencies can be independently adjusted by the choice of timing registers connected to pin 8 and 7 respectively. Resistor pin 8 is fixed which decides the mark frequency whereas resistor to pin 7 is variable which decides Space frequency, the output is phase continuous during transitions. The keying signal is applied to pin 9.

Description of Controls :

Frequency of operation is given as

$$fc = \frac{1}{RC} \text{ Hz}$$

R is either R_1 or R_2 and can be adjusted.

Assume a simple disc capacitor is used

$C = 0.1\ \mu F.$

suppose we want to generate two frequencies 2 kHz – 2.2 kHz. Then the frequency of operation or center frequency has to be select 2.1 kHz.

Output voltage / amplitude

1 kΩ = 60 mV

47 kΩ = onput voltage

Output voltage = 2820 mV

= 2.820 V

(In the receiver part at this frequency i.e. 2.1 kHz PLL will set or locked)

Now the center frequency

$fc = \frac{1}{RC}$ Hz

$2.1 \text{ kHz} = \frac{1}{R..0.1\ \mu F}$.

$R = 2.1*10^{3}*0.1*10^{-6}$

= 4.76 kΩ

So timing resistor is connected to pin 7 (variable) and pin 8(fixed) will be of value 4.7 kΩ. From graph of timing resistor Vs oscillation frequency this value of timing resistor 4.7 kΩ at at 2.1 kHz lies in the typical value range.

Frequency shift and modulation

I_T = 6 mA

$f = \frac{320\ I_T(mA)\ Hz}{C(\mu F)}$

= 19200 Hz

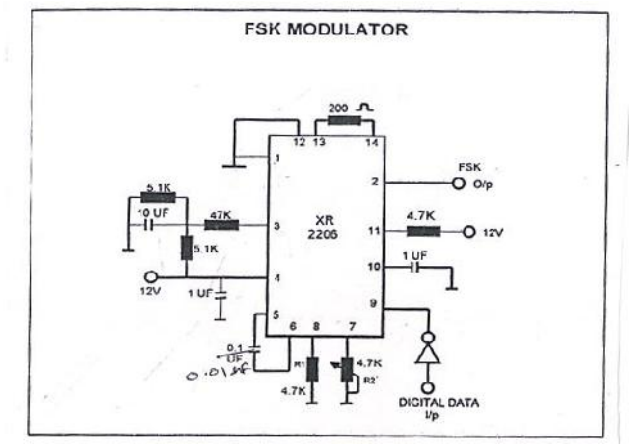


Fig. 2

4)FM TRANSMITTER

Basically there are three RF stages in FM transmitter. First stage is variable frequency VHF oscillator (frequency range of 88 MHz to 108 MHz) second stage is class C driver stage and final third stage is class C power amplifier stage. It can deliver upto 1 W RF power. With 70 cm telescopic antenna range of this transmitter is 1 KM. Now to transmit 90 MHz frequency the inductor and capacitor values are selected as follows :

$f = \frac{1}{2*3.14*\sqrt{LC}}$.

$90 \text{ MHz} = \frac{1}{2*3.14*\sqrt{LC}}$.

$\sqrt{LC} = \frac{1}{2*3.14*90 \text{ MHz}}$.

$LC = 3.127*10_{-18}$

$L*2.2*10^{-12} = 3.127*10^{-18}$

L = 1.5 uH

Transistor Q_1 and Q_2 are used to generate VHF oscillations as well as FM modulation BC 547 is used as transistor Q_1 which is audio frequency bipolar transistor of electron series. Transistor Q_2 is C2570 which is high frequency bipolar transistor. Q_1 is used to couple audio frequency to reactance modulator and Q_2 is class CVHF generator which drives class C Q_3 RF power amplifier. Q_3 is a transistor.

2N 3866 which is a high frequency power transistor. Antenna is coupled to RF amplifier stage using LC circuit. Dipole antenna is used for FM transmission. The whole circuit works on +12V power supply.

Here transistor reactance modulator method is used. In the reactance modulator shown in figure on RC capacitive transistor reactance modulator operates on the Clapp-Gouriet oscillator. Any reactance modulator may be connected across the tank circuit of any LC oscillator (not crystal) with one provision. The oscillator used must not be one that requires two turned circuits for its operation such as the tuned base-tuned-collector oscillator. The Hardey and Colpitts oscillator (or Clapp-Gouriet) are most commonly used and each should be isolated with bμFfer. The RF chock shown in the circuit are used to isolate various points of the circuit for alternating current while still providing a DC path. [1]

5) TRANSMITTING ANTENNA

Dipole antenna is used for transmission. Thickness of the antenna is 6 mm and length of antenna is 20 cm. [1]

International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 9
September 2017

Academic Science

RECEIVER SECTION

1) RECEIVING ANTENNA

It is dipole antenna same as used for transmission. Thickness of the antenna is near about 6 mm. [1]

2)FM RECEIVER

Output from antenna is given to FM receiver which is designed using IC CXA1619BS. It requires a very small number of peripheral components. It has very low current consumption, for FM it is typically 5.8 mA. It has built in FM/AM select switch. It has large output of AF amplifier. Very low peripheral components are required for FM reception. Here FM section includes RF amplifier, mixer, oscillator (incorporating AFC variable capacitor). IF amplifier, quadrature detection, tuning LED driver. [1]

3)FSK DEMODULATOR :

Output of FM receiver is given to demodulator IC XR 2211, XR 2211 is a monolithic phase-locked loop (PLL) system especially designed for data communication applications. It operates over a wide frequency range i.e. 0.01 Hz to 300 kHz, and has wide supply voltage range of 0.45 to 20 V and a wide dynamic range 10 mV to 3 V.,excellent temperature stability. i.e. +/-50 ppm/ degree C. But TTL compatibility and FSK demodulation with carrier detection are the main features which are more important in this system. The circuit consist of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection and an FSK voltage comparator which provides FSK demodulation. External component used to independently set center frequency bandwidth and output delay. GHere being PLL system the frequency shift is usually accomplished by driving VCO with the binary data signal so that the two resulting frequencies correspond to logic ‘0’m and logic ‘1’ states of the binary data signal. The frequencies corresponds to logic ‘1’ and logic ‘0’ are commonly called as Mark and Space frequencies. Here at the input capacitive coupling is used to remove DC level. A signal appears at the input, the loop locks to the input frequency and tracks it in between two frequencies with a corresponding dc shift at the output. Here functions of various external components can be described as resistor Ro (18l amd [pt 47k) and capacitor Co(0.22 µF) set the PLL center frequency, resistor R_1 (200 kΩ) sets the system bandwidth, and capacitor C_1(0.0047µF) sets the loop filter time constant and the loop damping factor. R_f and (100 k) and C_f (0.0047µF) form a one pole post detection filter for the FSK data output. The resistor (510k) from pin 7 to 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Designing of components :

Now circuit can be tailored by the choice of key components R_0 R_1, C_0 C_1, and CF. For a given set of FSK mark and space frequencies different parameters can be calculated as follows :

1) The timing register R_0

The timing register R_0 should be in the range of 10 kΩ to 100 kΩ. The recommendaed value is R_0= 20 kΩ. The final value of R_0 is normally fine tuned with the series potentiometer R_x.

$R_0 = R_0 + R_x/2$

We have selected a potentiometer of value 4.7 kΩ. Then R_0 = 20 kΩ+4.7 kΩ/2

= 22.35 kΩ = 22.4 kΩ

So, as timing resistor R_0 a series combination of 18 kΩ (fixed) and 4.7 kΩ (pot) is used.

By adjusting the position of pot properly desired value of center frequency to which PLL has to be lock can be achieved with proper selection of capacitor, C_0

2) VCO frequency and timing capacitor C_0,

$f_0 = 1/[R_0*C_0]$

Now since the frequency of operation of XR 2202 i.e. FSK modulator is 2.1 kHz so PLL has to be locked or set of the same frequcncy. f_0 = 2.1 kHz

Now timing capacitor

$C_0 = 1/[R_0*f_0]$

= 1/{[18 kΩ+4.7 kΩ]*2.1 kHz}

= 0. 19 µF

Since all values except f_0 can be rounded to nearest standard value so a capacitor of a valuie 0.022 of selected as timing capacitor, C_0 , C_0 = 0.022 µF

3) R_1 to give desired tracking bandwidth we have loop tracking bandwidth.

= $[f_1-f_2]/f_0 = R_0/R$

$\Delta f = R_0*f_0/R = [19*10^3*2.1*10_3]/100*10^3]$

= 0.477 kHz

$R_1 = R_0 * f_0/[f_1-f_2]$ = 199.847 kΩ.

4) Selected value of C_1 to set loop damping C_1 :

$C_1 = [12520*C_r]/R_f*C^2]$

Normally C = 0.5 is recommended.

$C_1 = [1250*0.1*106]/[100*10^3*0.5*0.5]$

= 0.005 µF

After calculated value of C_1 can be rounded to a standard value of 0.0047 µF

C_1 = 0.0014 µF.

5) Internal reference voltage, Vref (measured at pin 10)

Vref = Vcc/2 – 650 mV

= $12/2 – 650 * 10^{-3}$ = 5.35 V

6) Data filter capacitance C_r

$C_r = 0.25[R_{sum}$*Baud rate] Where

$R_{sum} = [R_f+R_1]R_B]/[R_1+Rf+R_B]$

And baud rate is in 1/ seconds.

$R_{sum} = [(100+200)*10^3*510*10^3]$

$/[100+200+510]*10^3$

= 188.88 kΩ

$C_r=0.25/[188.88*10^3*0.3*10^3]$= 0.0044 µF

C_rm can be rounded to nearest standard value of 0.0047 µF

7) FSK data filter time constant t_f :

$T_f = [R_B*R_f*C_r]/[R_B+R_f]$

$=[510*10^3*100*10^3*0.0047*10^{-6}]/ [510+100]$ = 0.393msec.

8) Peak detector current I_A :

I_A=Vref/20000 = 5.35/20000 = 0.0002675^a

I_A = 0.270 mA

9) VCO Conversion gain K_0{K_0 is the amount of change in VCO frequency per unit of DC voltage change at pin 11}

$K_0 = -2*\Pi/[Vref*C_0*R_0]${[rad/sed]/V}

$K_0 = 2.4*10^3${[rad/sed]/V}

10. Loop phase detector conversion gain Kd :

[K_4 is the differential DC voltage across pin 10 and pin 11 per unit of phase error at phase detector input.]

$K_4 = Vref*R_1 / [10000* \Pi][V/Rad$

= [5.35*200*10*] = 34.076V/rad/

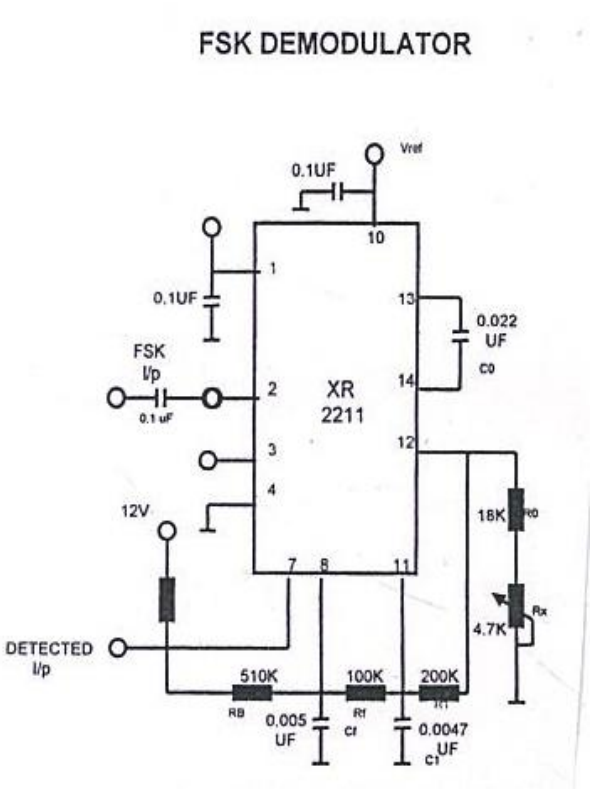


Fig.3

4) TTL TO RS 232 CONVERSION.

Output of FSK demodulator is given an input to IC 1488. R is 14 pin low power monolithic quad line driver using BiMos technology. The inputs feature TTL compatibility with minimum loading. The outputs feature internally controlled slew rate limiting, eliminating the need of external capacitors. Here, at input if Mark frequency i.e. logic '1' level is present then it is converted to -12 V and logic'0' i.e. Space frequency is converted to + 12 V at the output of IC 1488. This output is then given to the receiving PC.

Software:

The main program is written in 'C' language.

International Journal of Electronics, Electrical and Computational System
IJEECS
ISSN 2348-117X
Volume 6, Issue 9
September 2017

Academic Science

MAIN PROGRAM

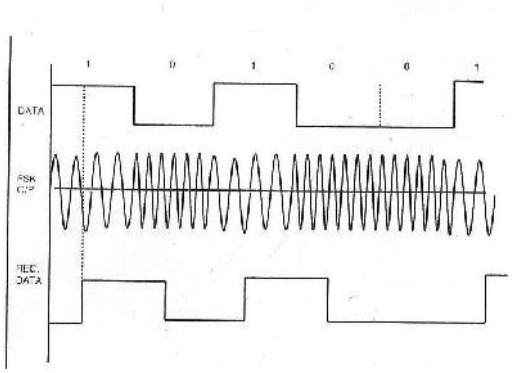
```
/*INCLUDE THE HEADER FILES*/
#include<stdio.h>
#include<conio.h>
#include<bios.h>
#include<dos.h>

/* INITIALISE THE PORT ADDRESS*/
# define port 0x3F8

/* MAIN FUNCTION STARTS*/
void main()
{
 int c,ch,i,j;
 char y,a;
 clrscr();

 /*CLEAR ALL THE BUFFERS*/
 flushall();

 /*ENTER OPTION FOR TRANSMISSION OR RECEPTION*/
 printf("\n PRESS '0' FOR TRANSMISSION & '1' FOR RECEPTION:");
 scanf("%c",&y);

 while(y=='0'||y=='1')
 {
     printf("\n*****************************\n");

 /*TRANSMITER LOOP STARTS*/
     while(y--'0')
     {
       c=getche();
 /*SEND THE ACTUAL DATA*/
       outportb(port,c);

 /*PRESS 'Tab' FOR CHANGING MODE OF OPERATION*/
       if(c==27)
       {
          y='1';
          printf("*\n CHANGING MODE OF OPERATION F
TRANSMITER TO RECEIVER*\n");
          break;
       }

 /*PRESS ' ~ ' FOR ENDING THE COMMUNICATION OR CONTINUA'
OF RECEPTION*/
       while(c==126)
```

```
{
 /*CHECK THE 'DR' BIT OF 'LSR' IN UART*/
          i=inportb(port+5);
          if(i&1)
          {
           j=inportb(port);
           if(j=='y'||j=='Y')
           {
            y='E';
            printf("\n *END OF TANSMISSION* \n");
            break;
           }
           else if(j=='n'||j=='N')
           {
            y='1';
            printf("*\n WANT TO CONTINUE* \n");
            break;
           }
          }
       }
 /*TRANSMITER LOOP ENDS*/

     printf("\n*****************************\n");

 /*RECEIVER LOOP STARTS*/
     while(y=='1')
     {
 /*CHECK THE "DR' BIT OF 'LSR' IN UART*/
       i=inportb(port+5);
       if(i&1)
       {
 /*RECEIVE THE ACTUAL DATA*/
        ch=inportb(port);
        printf("%c",ch);

 /*LOOP FOR CHANGING OF MODE OF OPERATION*/
        if(ch==27)
        {
          y='0';
          printf("\n*CHANGING MODE OF OPERATION FROM
RECEIVER TO TRANSMITER*\n");
          break;
        }

 /*LOOP FOR END OF COMMUNICATION OR CONTINUATION OF
TRANSMISSION*/
        while(ch==126)
```

```
{
          printf("\n DO YOU WANT TO END TRANSMISSION:(y/n):>")
          a=getche();
          if(a=='y'||a=='Y')
          {
           outportb(port,a);
           y='E';
           printf("\n *END OF TRANSMISSION* \n");
           break;
          }
          else if(a=='n'|a=='N')
          {
           outportb(port,a);
           y='0';
           break;
          }
        }
      }
     }

     /*LOOP FOR END OF COMMUNICATION*/
     if(y=='E')
     {
       printf("\n*****************************\n");
       break;
     }
 }
 getch();
}
```

Result:

The transmitted and received data



References :

1.Electronic Communication Systems
– Kennedy and Devis.
Tata Magraw Hill Publications. 4th Edn.
2.Opams and Linear Integrated Circuits
- Ramakant Gaikwad
3. IBM PC and Clones.
- Govindarajalu.
4. datasheetcatalog.com